UNIVERSITY OF CALIFORNIA

Santa Barbara

Any-point bias control of Mach-Zehnder modulators using digital filters

A Thesis submitted in partial satisfaction of the

requirements for the degree Master of Science

in Electrical and Computer Engineering

by

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Professor Jonathan Klamkin

June 2017

The thesis of Hector Andrade is approved.

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Clint Schow

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James Buckwalter, Committee Chair

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ACKNOWLEDGEMENTS

I would like to thank my M.S. and future Ph.D. advisor, Professor James Buckwalter, for all his patience and advice these last months. I am also grateful to Dr. Roger Helkey for his valuable suggestions, as well as Rui-Lin Chao and Aditya Jain for their assistance with the setup. I am also thankful to my future Ph.D. advisor, Professor Clint Schow and Professor Jonathan Klamkin for agreeing to be a part of the thesis committee.

I would like to dedicate this thesis to my girlfriend Olga for all her encouragement during the past two years and to my parents Héctor and María Esther, and my brother Roberto for their lifelong support.

ABSTRACT

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Feedback control is used to maintain Mach-Zehnder modulators at a desired bias point, since heating and aging effects in its electro-optic materials cause a drift in its transfer function over time. Considering that the desired bias point in the MZM transfer curve varies among different applications, the control method should have an adjustable setpoint. The proposed method seeks to achieve this with the minimum number of components possible.

SIMULINK models were used to obtain a better understanding of MZM biasing. Then, after comparing available commercial products and a literature review, it was decided to apply a known technique whereby a low-frequency dither signal is applied to the MZM DC input, the output of the MZM is measured and a PID controller adjusts the MZM DC voltage to maintain a constant ratio of the dither tone's 2nd harmonic and fundamental. This method is independent of optical power and allows the bias to be set to any point in the transfer curve.

To eliminate the need for standalone filters for each frequency and an additional IC for obtaining the power ratio, digital filtering, processing and PID control are all done within a microcontroller. A prototype board was built and the bias control measurements are presented.

The application of this method to Si MZM is also briefly discussed.

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1. Introduction

A. Analog optical links

Optical links are used to convey an electrical signal over an optical carrier. Analog optical links are those in which optical modulation depth is sufficiently small that small-signal analysis is possible, as opposed to digital optical links, where modulation depth approaches 100% [1]. Although the great majority of fiber optic links in use are digital, there are some applications, such as antenna remoting [2] [3], where analog fiber optic links are employed.

In its simplest form, an analog optical link consists of three elements, an electrical-to-optical converter, an optical transmission medium and an optical-to-electrical converter, as depicted in Figure 1.

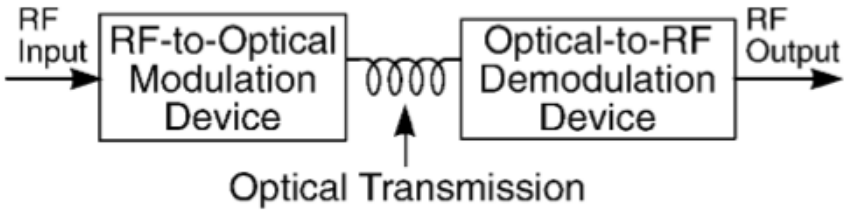


Figure 1. Basic components of an analog fiber optic link [4]

Electrical-to-optical converters make use of electro-optic effects, by which changes in the refractive index of a material are induced by the application of an external electric field. This process is known as modulation of the optical signal, and therefore electrical-to-optical converters are commonly known are modulators.

B. Mach-Zehnder modulator

One of the most popular modulators is the Mach-Zehnder modulator (MZM), which employs interference to convert phase shift into amplitude variation. As shown in Figure 2, incoming light is split equally into two arms, across which opposite electric fields are applied. This causes a phase difference between the light waves traveling in each arm, which interfere when combined at the output. In an ideal MZM the resulting power of the output signal will range from 0 to the total input power depending on the magnitude of the electric field. The two waves interfere destructively when the phase shift is a multiple of π and constructively for multiples of 2π.

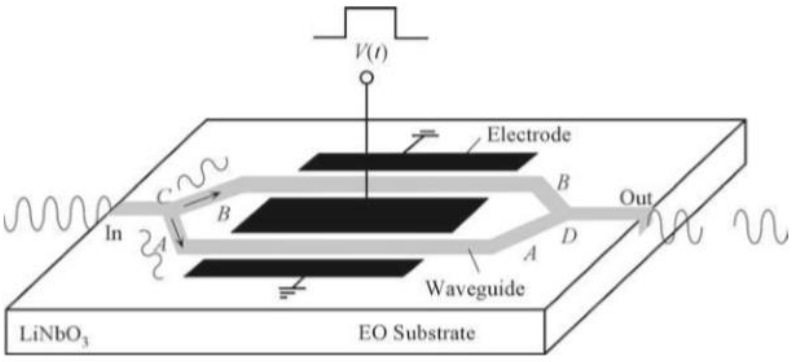


Figure 2. Mach-Zehnder modulator [5]

The resulting power transfer function of the MZM is a raised cosine, shown in Figure 3. The transfer function in its simplest form can be expressed as

$$P_{out} = \frac{P_{out,max}}{2} [1 + cos(\theta)] \quad (1.1)$$

where θ is the phase difference between the two interfering light waves. A useful parameter is V_π, the voltage at which the phase difference between the two arms is 90°, and

thus the output power of the MZM is 0.

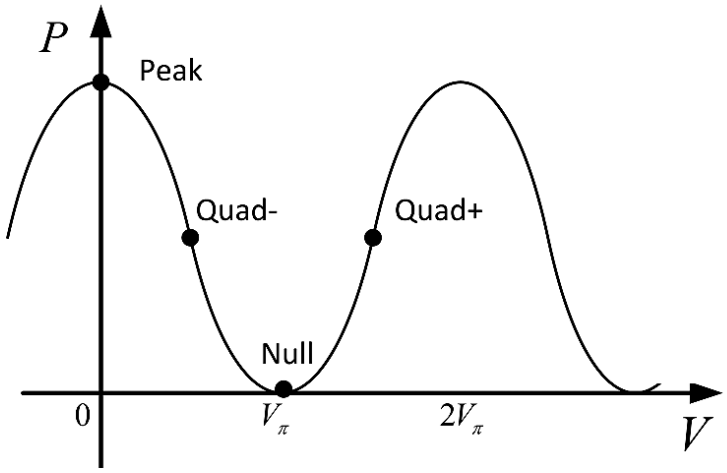


Figure 3. MZM power transfer function with common bias points. "Quad" stands for "quadrature" [6]

C. MZM bias control

1. MZM biasing

A DC voltage is usually applied to MZMs to operate at a desired point in the transfer curve. It can be observed in Figure 3 that the quadrature (half-power) points, at 90° and 270° ($\pi/2$ and $3\pi/2$), are the most linear. This is in line with small-angle approximation, since $\cos(\pi/2) = \sin(0)$ and $\sin(\theta) \approx \theta$. In most analog optical link applications, this is the optimum bias point, since commonly the objective is to minimize the 2nd order harmonic distortion (HD2) and thus maximize the dynamic range of the link. Figure 4 shows the fundamental, HD2 and 3rd order distortion (HD3) products at the output of the MZM as a function of bias point. It is evident that at 90° ($V_\pi/2$) the fundamental signal is greatest and HD2 is eliminated.

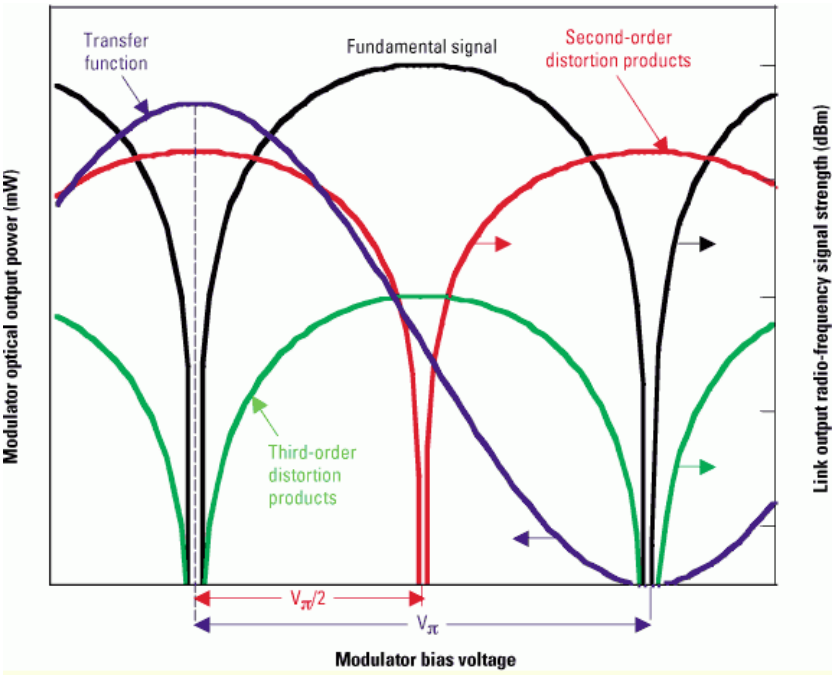


Figure 4. MZM transfer function (purple), and link output power at fundamental (black), 2nd harmonic (red) and 3rd harmonic (green) [7]

There are techniques such as frequency conversion, however, that exploit the nonlinearity of the MZM at other bias points. Reverting to small-angle approximation, nonlinear behavior is attained at the null and peak bias points (0 and π), since $\cos(0) \approx 1 - \theta^2/2$. Frequency conversion can be employed to reduce front-end hardware complexity of antenna systems and efficiently extend link frequency coverage into the millimeter-wave (MMW, 30–300 GHz) range [8]. As shown in Figure 5, this is achieved by adding an information-bearing RF signal at f_{RF} to a local oscillator signal at f_{LO}. The resulting up-converted signal is then at $f_{IF}=f_{RF}\pm f_{LO}$.

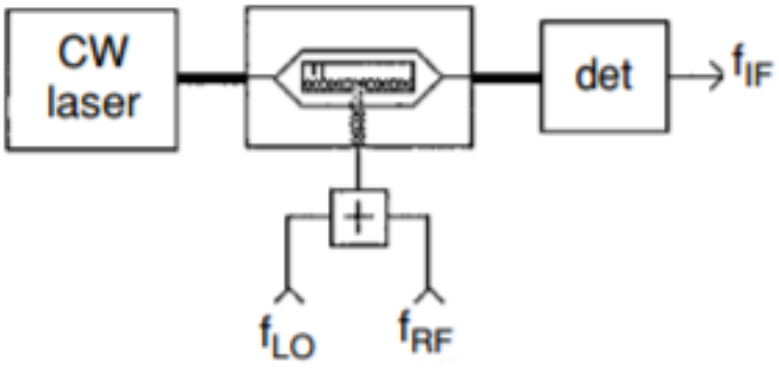


Figure 5. MZM frequency conversion [8]

In addition to quadrature and peak/null biasing, there are techniques that require biasing at other points in the transfer function. In sub-octave links that can be maintained at the relative intensity noise (RIN) limit or detector saturation limit using a lower Mach-Zehnder bias, a larger dynamic range can be achieved [9]. Figure 6 depicts third-order intermodulation distortion (IM3) curves for an MZM at both 50% bias (quadrature) and 5% bias (18°). It can be observed that at lower bias third-order intermodulation (IM3) suppression is higher, and that as optical modulation depth (OMD) increases, the noise floor falls relative to the carrier signal. The highest dynamic range is then found where the low bias IM3 tone coincides with the noise floor, obtaining an improvement of 8.5dB with respect to quadrature biasing. It is important to reiterate that this technique is intended for sub-octave links, since it suppresses IM3 by operating at a more quadratic region of the transfer curve, which in turn increases HD2 terms. Figure 7 illustrates the relevant distortion tones in sub-octave links.

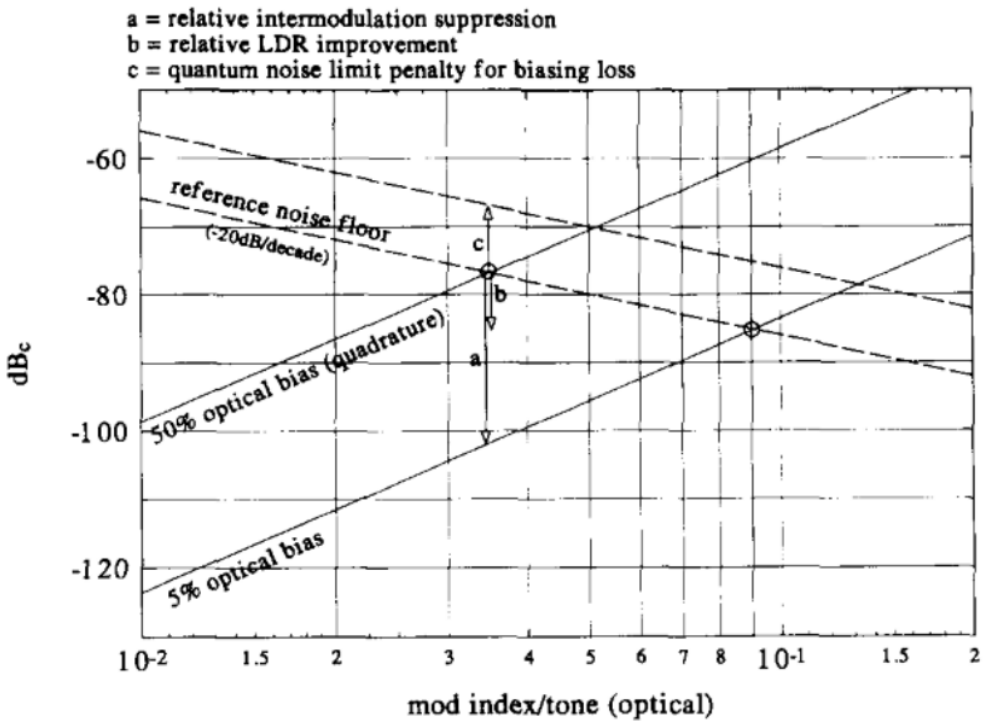


Figure 6. Third-order intermodulation distortion for a Mach-Zehnder conventionally biased to 50% and low biased to 5% vs OMD

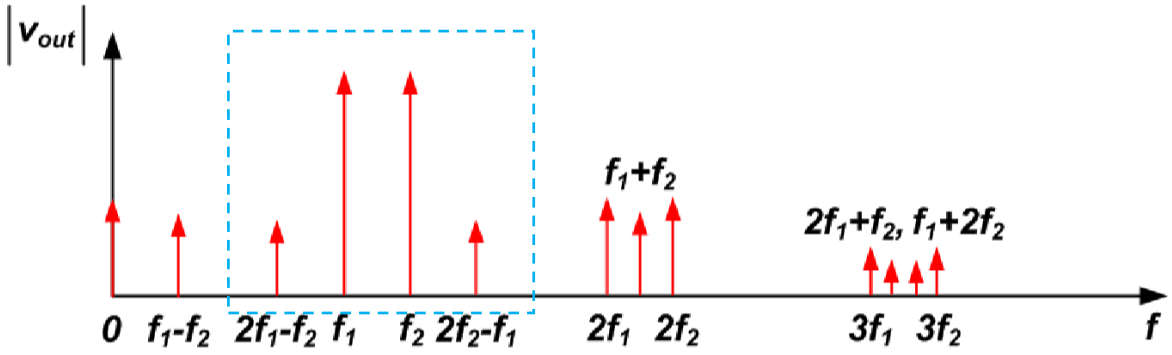


Figure 7. Picture of distortion generated from two tones. The dashed box indicates the relevant components in sub-octave links [10]

2. Feedback control of MZM bias

Pyroelectric, photorefractive, and photoconductive effects in the MZM's electro-optic material cause the MZM transfer function to "drift" to the left or right-as depicted in Figure 8 [11]. This makes the use of closed-loop control necessary to maintain a desired bias point, which is most commonly implemented via proportional-integral-derivative (PID) control [6] [12]. The drift is a relatively slow process than can be measured in seconds or even minutes and thus the PID loop cycle can be equally lengthy without affecting the performance of the analog link.

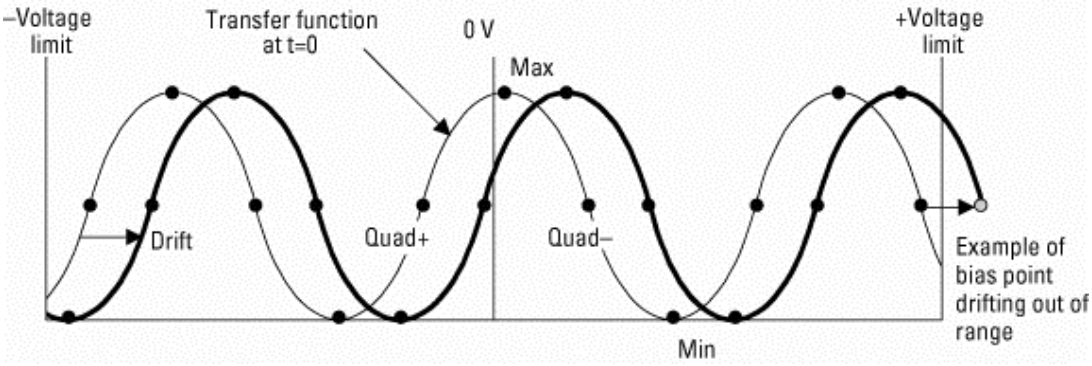


Figure 8. Effect of MZM bias drift [11]

2. SIMULINK models

A. Time domain model

Initially, the time domain model shown in Figure 9 was created to better understand the MZM behavior at different bias points. As described in the previous chapter, the input laser signal is split, with half of the power going to each MZM arm. The electrical RF signal and bias voltage induce an opposite phase shift in each arm and the optical signal is recombined at the output and $\pi/2V_\pi$ is effectively the conversion factor from input voltage to phase shift in each arm.

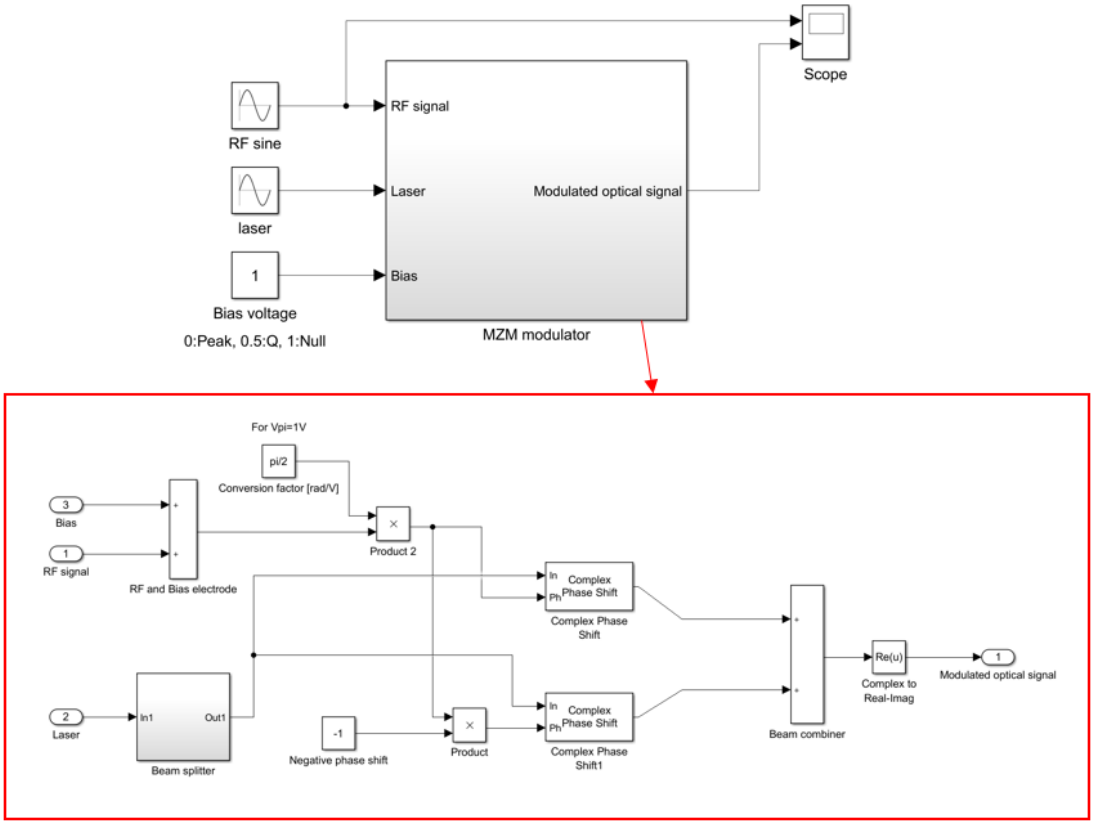


Figure 9. SIMULINK MZM time domain model

An amplitude modulation (AM) simulation was done at three different bias points. Figure 10 shows the time domain RF input and optical output. The RF amplitude is 10% of V_π.

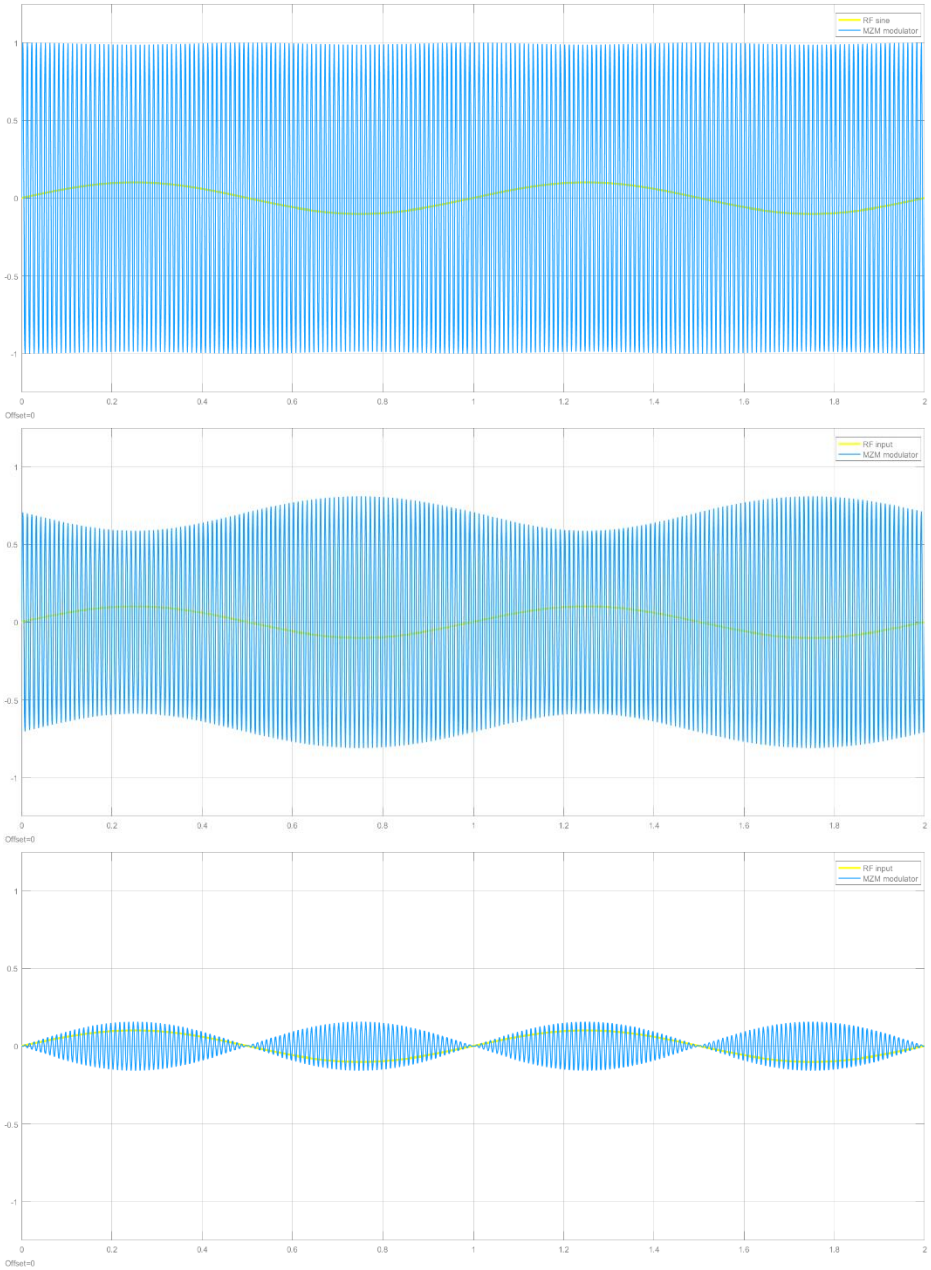


Figure 10. MZM time-domain RF input signal (yellow) and optical output signal (blue), at peak bias (top), quadrature bias (middle) and null bias (bottom). Units on both axes are arbitrary.

At null and peak bias, it can be noticed that the period of the output signal envelope is twice that of the RF signal. The fact that the 2nd-order component dominates, agrees with the

expected quadratic behavior at these bias points. At quadrature, the modulation is linear and there is a 180° phase between RF input and the output signal envelope, which is in line with the first quadrature bias point shown in Figure 3.

B. Frequency domain model

As will be described in chapter 3, a dither signal is commonly used to perturb the MZM bias operating point to determine the location of said point on the transfer function. A model (Figure 11)Figure 11. SIMULINK frequency domain model was created to predict the output spectrum with different waveforms. A low-pass filter (LPF) was added before the MZM to reduce the magnitude of harmonics of the dither signal.

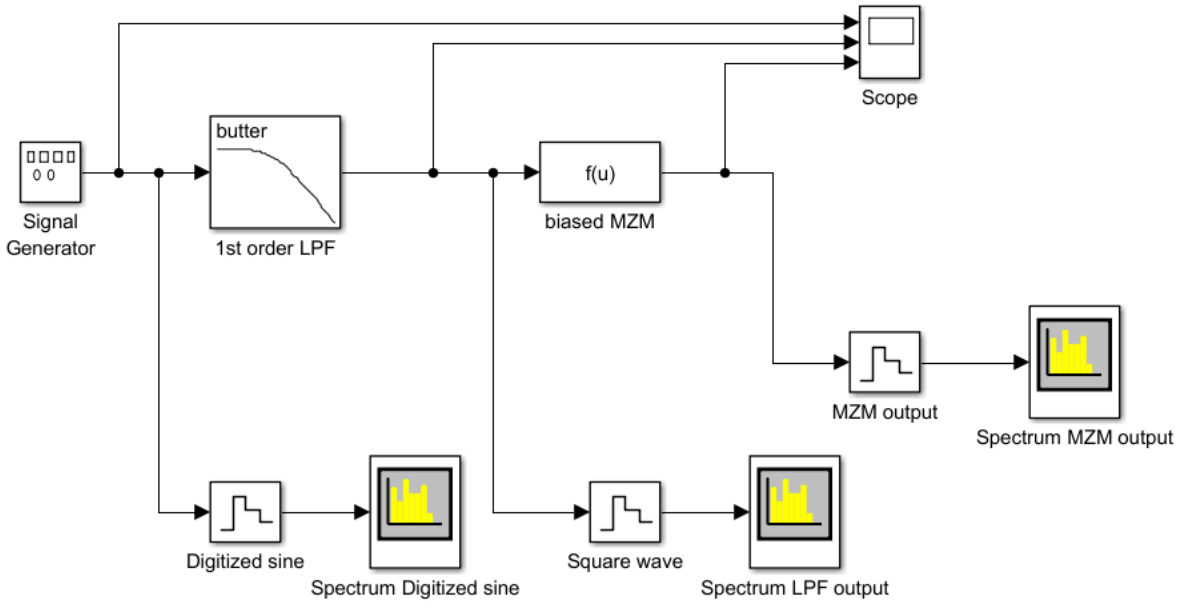


Figure 11. SIMULINK frequency domain model

First, a 1kHz ideal sine wave dither signal was simulated (results shown in Figure 12). The continuous time results coincide with the AM simulations shown above. As expected, the

MZM produces HD3 and suppresses HD2 at quadrature, and has the opposite effect at null bias.

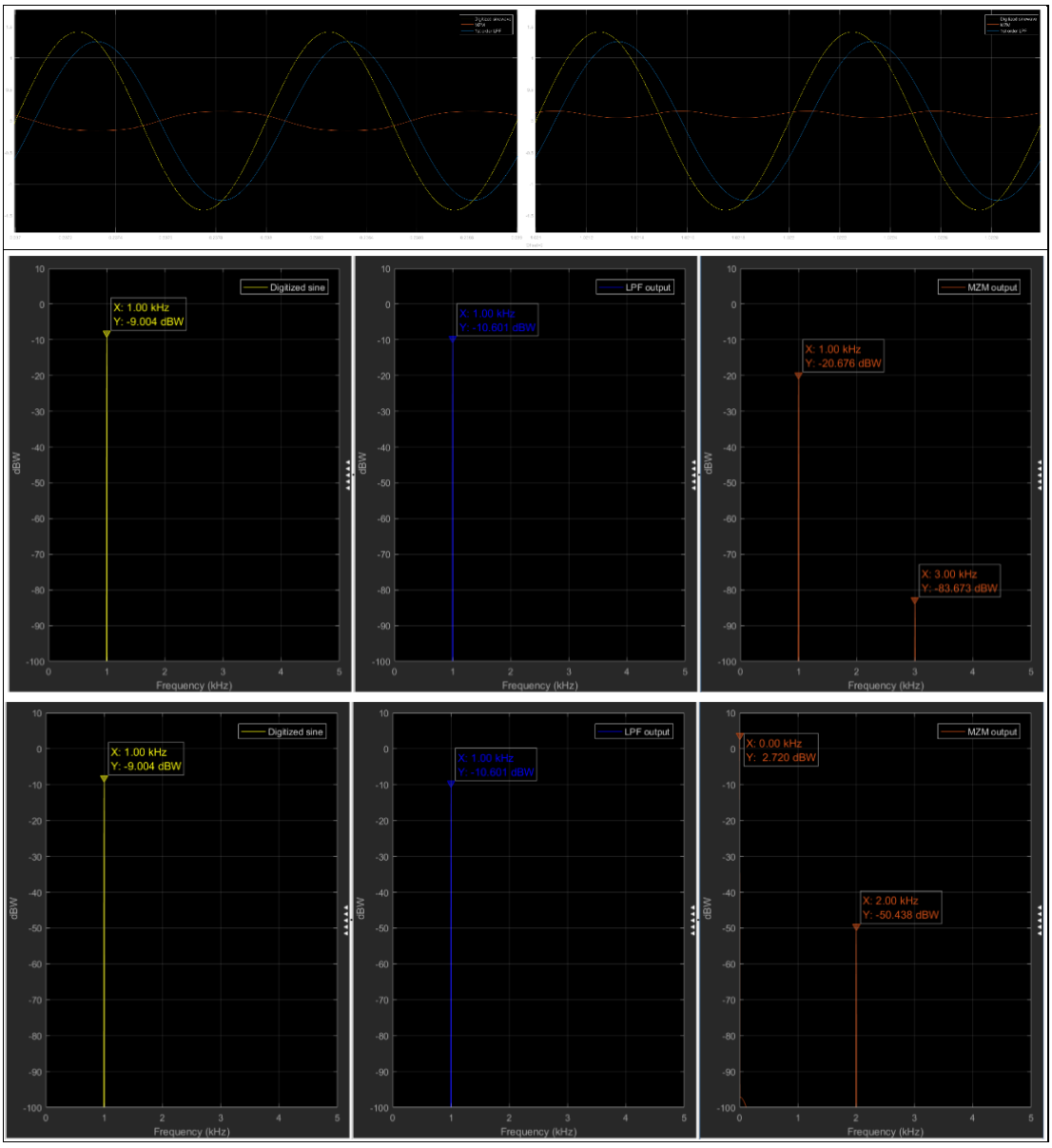


Figure 12. Simulation of ideal sine dither. Top: time domain simulation of RF signal (yellow), LPF output (blue) and MZM output (orange) at quadrature bias (left) and null bias (right). Middle: frequency spectrum at quadrature bias. Bottom: frequency spectrum at null bias.

Since the dither signal may be generated using a digital-to-analog converter (DAC), it is informative to simulate a discrete sine wave. Figure 13 shows the results for a 10-point digital sine wave dither. Although even and odd-order harmonics are introduced, this should not

hinder the bias control method, since the output spectrum can be filtered to obtain the desired frequency components. However, due to nonlinearities of the MZM, these additional components may appear as sidebands within the RF spectrum.

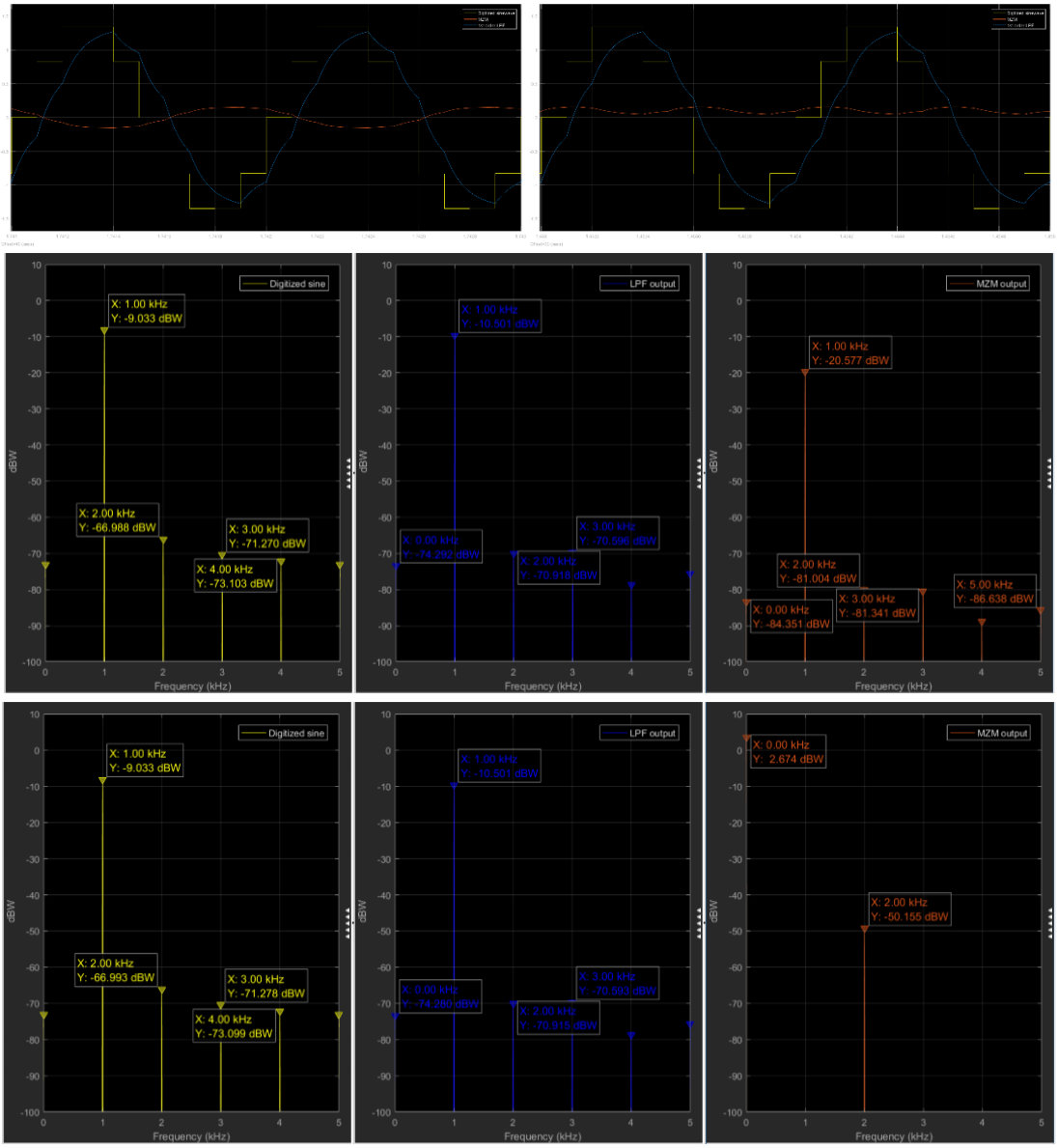


Figure 13. Simulation of 10-point digital sine dither. Top: time domain simulation of RF signal (yellow), LPF output (blue) and MZM output (orange) at quadrature bias (left) and null bias (right). Middle: frequency spectrum at quadrature bias. Bottom: frequency spectrum at null bias.

3. MZM bias control methods

A. "Photonic Analog Link on Si" project objectives

The work described in this thesis was done as part of the "Integrated Photonic Analog Link on Si" project at the Institute for Energy Efficiency at UCSB. The success criteria for the bias control was to ensure < 0.1° bias point error in a volume of less than $1cm^3$ and the desired bias point was not defined. A comparison of compact commercial off-the-shelf (COTS) MZM bias controllers was done to determine if the success criteria could be met. This is shown in Table 1. It can be noted that the dimension, bias error and bias point criteria are not met by available products. At this point a literature review was done to determine the ideal bias control method to employ.

Table 1. Comparison of compact COTS MZM bias controllers [7] [13] [14].

Parameter / Characteristic	**Project goal**	**Option 1: Photonics Systems Inc. PSI-2011-11**	**Option 2: Pharad MBC-DF-UC-U**	**Option 3: YY Labs Inc. 0090-2**
Dimensions	$<1cm^3$	4.2cm x 1.1cm x 1.3cm = $6cm^3$	5.1cm x 6.4cm x 0.9cm = $29.4cm^3$	4.6cm x 2.0cm x 1.3cm = $12cm^3$
Bias point	Adjustable	Fixed (Peak/null or Quadrature)	Fixed (Peak/null or Quadrature)	Fixed (Peak/null or Quadrature)
Bias point error	<0.1°	<1°	<1°	<3°
Dither/Ditherless		Dither	Ditherless	Dither

B. Literature review

From the early 1990s closed-loop methods for MZM bias control have been patented and published in research articles.

1. Patents

The patent "Modulator-based Lightwave Transmitter" [15] describes a closed-loop bias

control method for MZMs. In this approach, shown in Figure 14, the controller contains a reference signal (dither) that operates as a predetermined frequency which amplitude-modulates the electrical data signal that goes to the input of the MZM. The MZM output optical signal is then sent to a photodetector (PD) and the phase of the reconstructed output electrical signal is compared to the phase of the dither signal, with the phase difference being zero at the quadrature point. The bias voltage is then continuously corrected by integrating the error. This technique demonstrates that it is necessary only to measure the output signal of the MZM to determine the phase bias, which is an important advantage of a dither-based approach.

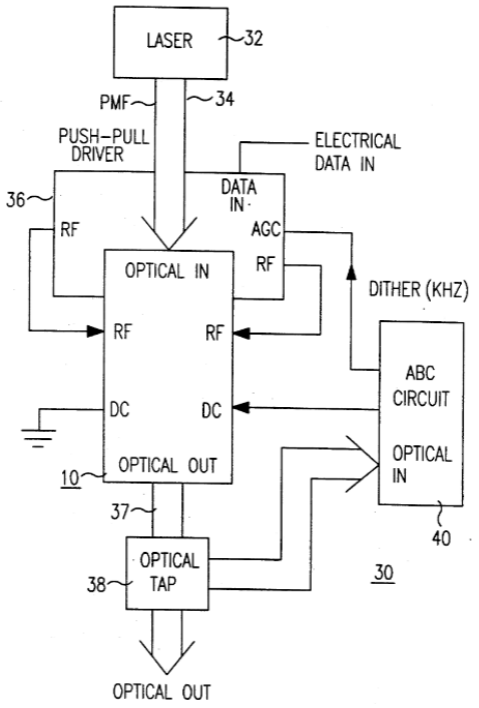


Figure 14. Automatic bias control by dither phase comparison

Another patented approach for locking to the half-power point consists in modulating a time-varying signal on and off at a modulation frequency f_m that is much lower than the

frequency components within the spectrum of a time varying signal (dither), such that energy within the time varying signal spectrum is recovered at the modulation frequency when the modulator is not operating at the half-power point. Due to the second order response of the modulator at any point except quadrature, energy within the dither signal spectrum is recovered at f_m if the modulator is not operating at that point. A phase sensitive demodulator retrieves the signal indicative of the modulator optical output signal to provide a DC voltage signal value indicative of the half-power point bias error value, which is then integrated to obtain the bias voltage value. This method is depicted in Figure 15 and Figure 16.

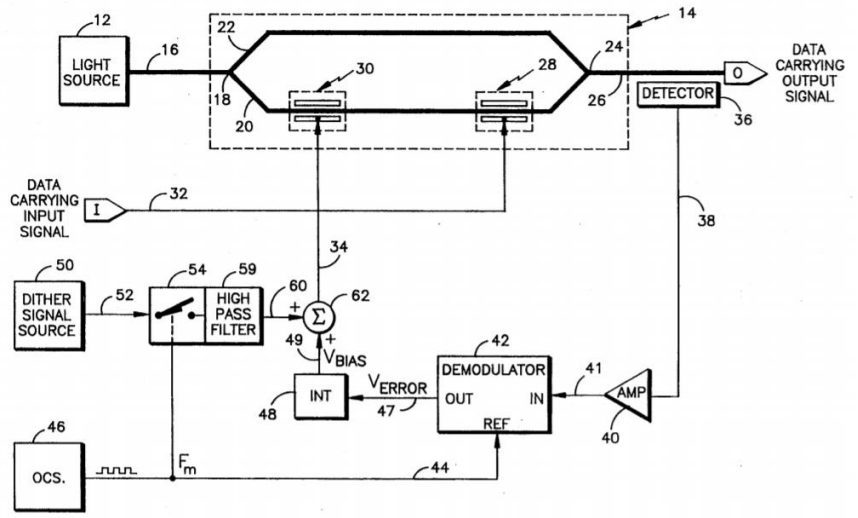


Figure 15. Gated-dither bias control of MZM

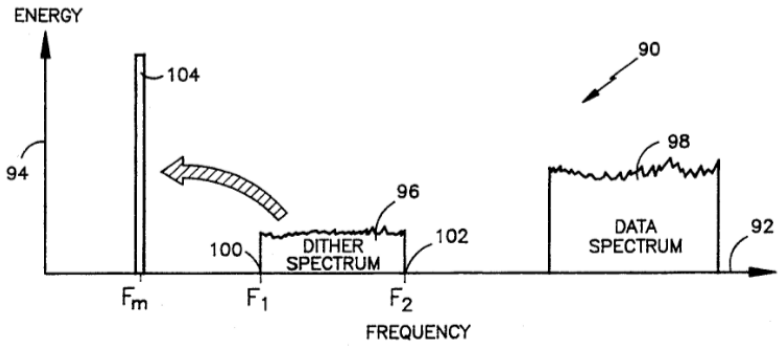


Figure 16. Spectrum of data-carrying signal, dither signal and modulation signal

More recent patents also make use of a dither signal to lock to the desired bias point [16] [17].

2. Articles

As is mentioned in the introduction, the desired bias phase will depend on the analog optical link where the MZM is to be employed. This means that a bias control method that allows for locking at any point on the MZM transfer curve is very advantageous. One such approach utilizes the ratio of the first harmonic of a dither signal and the average MZM output power [12]. Figure 17 shows a simulation of the output dither magnitude and its average power as a function of bias phase, where negative magnitude values refer to the sign of the phase with respect to the input dither signal. The ratio (red curve) is injective from 0 to 360°, which allows for locking at any point in the transfer function. As illustrated in Figure 18, a low-frequency dither is applied to the modulator bias and a small fraction of the output is tapped and directed to a low-pass filter (LPF) to eliminate the RF data signal components. The optical signal is then sent to a PD, where the DC output is proportional to the average power and the AC output is the dither signal. Another benefit of this technique is that it is independent of the

MZM input optical power, i.e., laser power fluctuations.

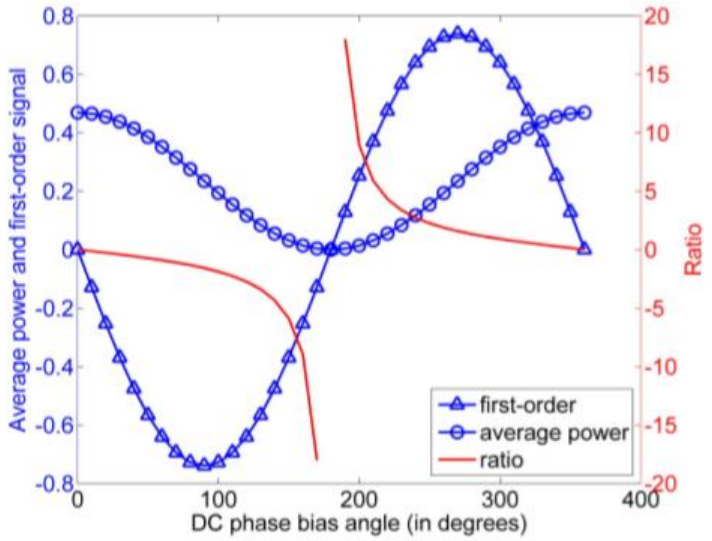


Figure 17. Simulated first-order harmonic (triangle) and average power (circle) from the photodiode and their ratio (smooth line) as a function of phase bias angle.

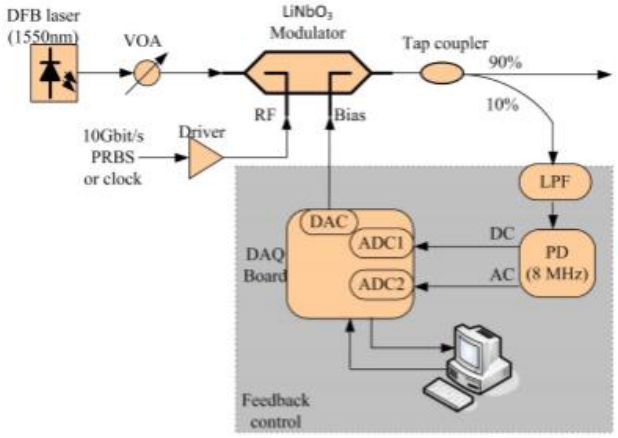


Figure 18. Dither average power ratio MZM bias control setup

Another control method for locking to any bias point consists in measuring the ratio of the first and second harmonics of a dither tone at the output of the MZM to determine the bias error [18]. The simulated values of the first and second harmonics of the dither as a function of phase bias can be seen in Figure 19. It can be observed that the ratio is injective for 0 to

180°, and thus can be employed as a control process variable for any bias point in that range. The setup that was used, shown in Figure 20, employs two bandpass filters and a log amp ratio divider to obtain the ratio. A PID controller is implemented within a microcontroller, which outputs a DC voltage that is combined with the dither signal before being input to the MZM.

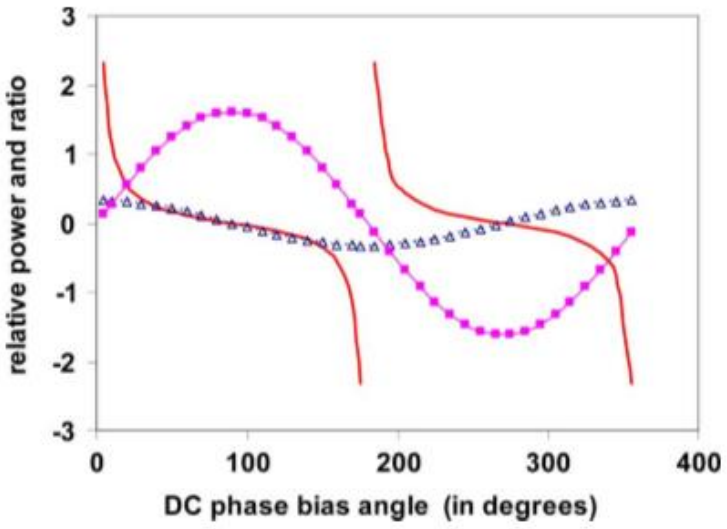


Figure 19. Simulated 2nd-order harmonic (triangle) and first order (square) signals from the photodiode and their ratio (smooth line) as a function of phase bias angle. Negative and positive signs of the signals correspond to phase changes relative to the input

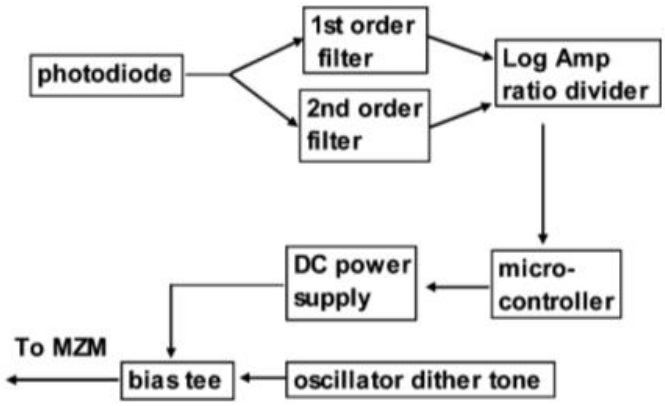


Figure 20. 2nd to first harmonic dither ratio bias control setup

4. Project proposal and setup

A. Project proposal

After the literature review and considering the project goals mentioned in section 2.A, it was proposed to employ the known technique that utilizes the ratio of HD2 and fundamental of a dither signal. Instead of using standalone filters for each frequency and an additional logarithmic amplifier IC as in [18], digital filters would be implemented within a microcontroller to minimize the dimensions of the bias controller. A schematic of the proposed closed-loop control is shown in Figure 21.

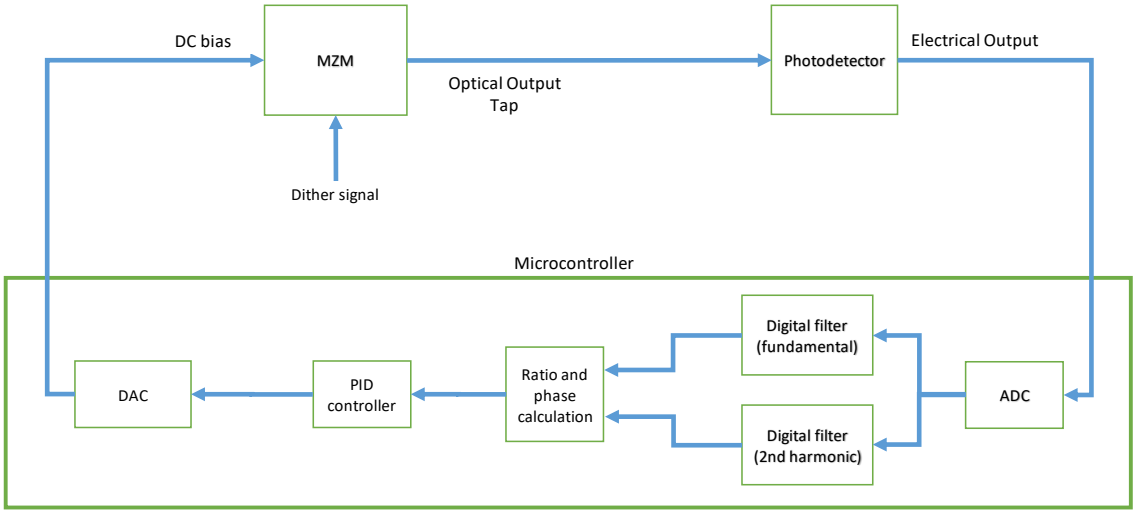


Figure 21. Schematic of proposed bias control loop

B. Bias controller setup

1. Microcontroller choice

After an extensive product search, it was decided to implement the bias controller on the FRDM-KL25Z development platform (Figure 22) for the NXP MKL25Z128VLK4

microcontroller, which has integrated 16-bit analog-to-digital converters (ADC) and a 12-bit DAC. This evaluation board has a built-in debug interface for flash programming and is enabled for the ARM mbed platform, which provides an online C/C++ compiler, all of which greatly facilitate the coding process.

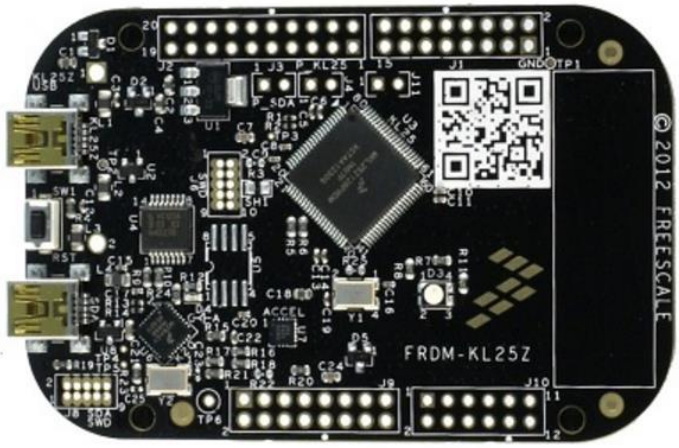


Figure 22. FRDM-KL25Z development platform

2. Components

The bias control loop was set up using commercially available components, which are listed in Table 2.

Table 2. Components used in bias control setup

Component	Model	Description	Specifications
MZM	JDSU APE	20GHz, 1550nm analog intensity modulator	Bias Vπ = 12V
Photodetector	THORLABS DET01CFC	Fiber Input InGaAs Biased Detector	Peak λ = 1550nm Responsivity at 1550nm = 0.95 A/W Output voltage = 0 to 10V (High Z)
Laser	QDFBLD-1550-100	Wavelength stabilized single mode fiber coupled laser diode	45mW @ 1550nm
Laser current source	LDX-3500B Series	Precision Current Sources	Output current range: 200mA
Microcontroller development platform	FRDM-KL25Z	Microcontroller board for easy access to to I/O	ADC, DAC range: 0 - 3.3V

3. Electrical network

Since the MZM V_π = 12V and the microcontroller's ADC and DAC range is only 3.3V, it was necessary to add an electrical network (Figure 23). A summing amplifier is used to add the dither signal to the DC bias voltage generated by the DAC prior to the bias port of the MZM. At the MZM output, a LPF reduces noise above the dither's 2nd harmonic and a high pass filter (HPF) removes the DC component. A tunable offset is then added and the signal is adjusted to utilize the full scale of the microcontroller's ADC by another summing amplifier.

The circuit was built initially using a breadboard and then an RF prototype (Figure 24) was constructed on a duroid board with a copper ground plane on one side. Microstrip was used for the signal traces and aluminum launcher blocks were used to place SMA connectors. These connectors were used to interface with the PD and MZM bias port. An Op Amp IC (ALD2702) was used for the summing amplifiers.

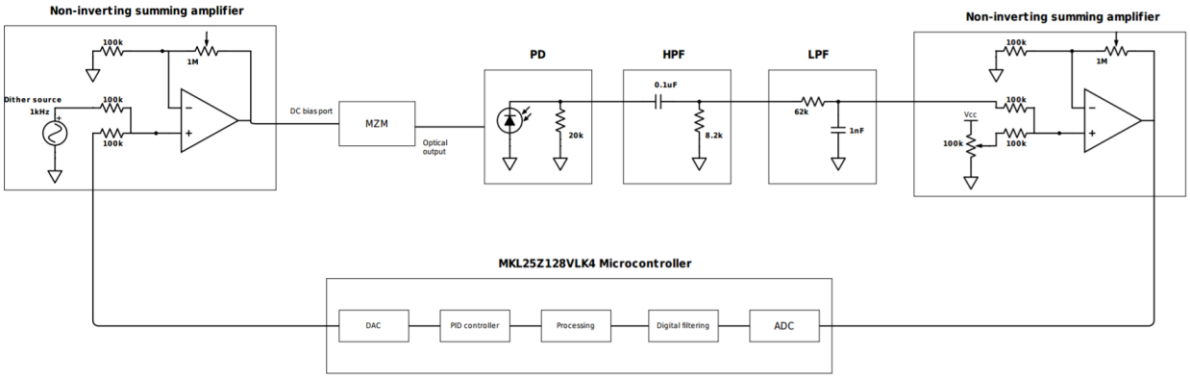


Figure 23. Schematic of MZM bias control loop (this project)

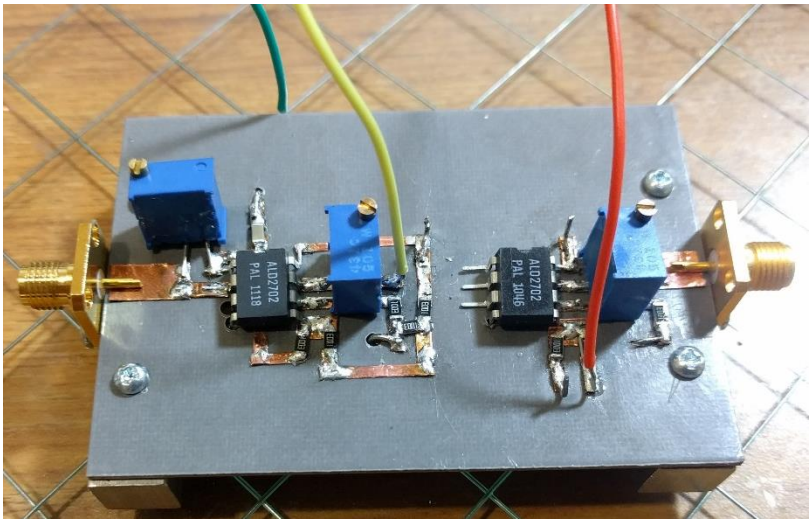


Figure 24. RF prototype of electrical network for MZM bias controller

C. Noise analysis

The average error of the bias phase of the controller is determined by the root mean square (RMS) noise of the dither fundamental and 2nd harmonic measurements within the microcontroller. The noise analysis was carried out for two sources, the electrical network and the quantization noise of the ADC.

1. Electrical network noise

Noise analysis of the circuit was done on LTSPICE, which considers shot, thermal and flicker noise [19]. The MZM and PD were modeled as a voltage controlled current source, with the PD junction capacitance and shunt resistance values taken from the PD datasheet. Figure 25 shows the circuit schematic, the transient analysis and the noise analysis. It can be seen in the transient analysis that the output signal, which is read by the ADC, utilizes most

of the 3.3V range. The integrated spectral noise density $V_{electricalnoise,RMS}$ is 124.9μV.

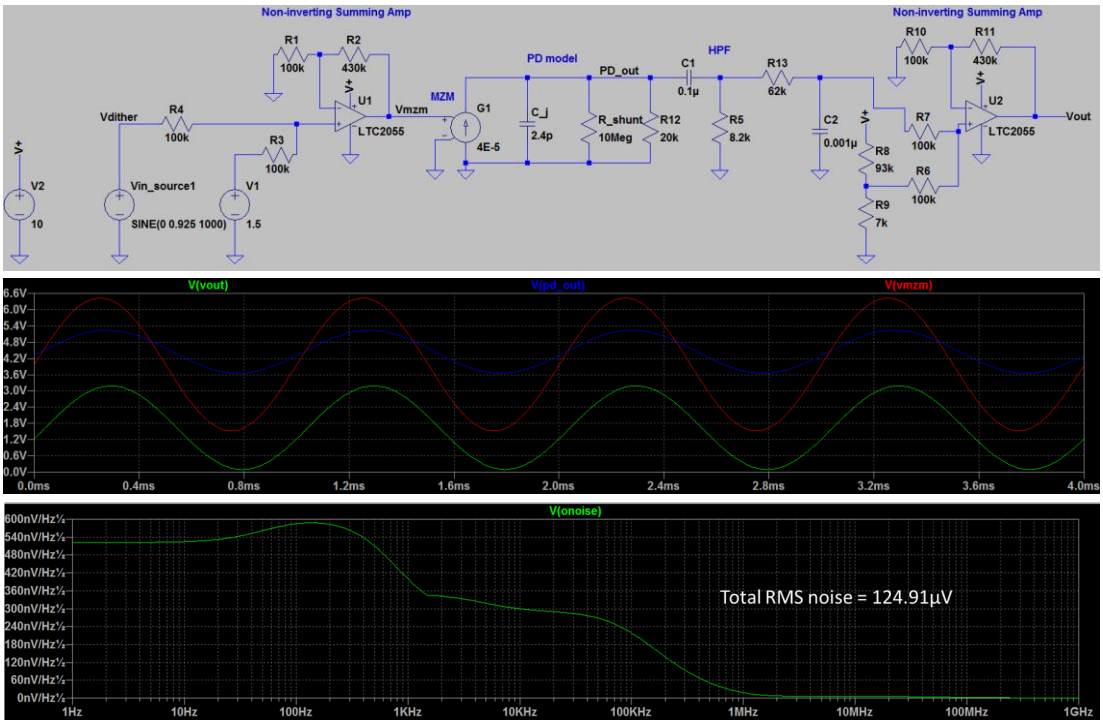


Figure 25. SPICE analysis of electrical network

2. Quantization noise

Quantization noise in ADCs is a result of rounding errors and thus decreases as resolution increases. The quantization error can be approximated by a sawtooth waveform [20], where the maximum error value is ± ½ LSB, as illustrated in Figure 26.

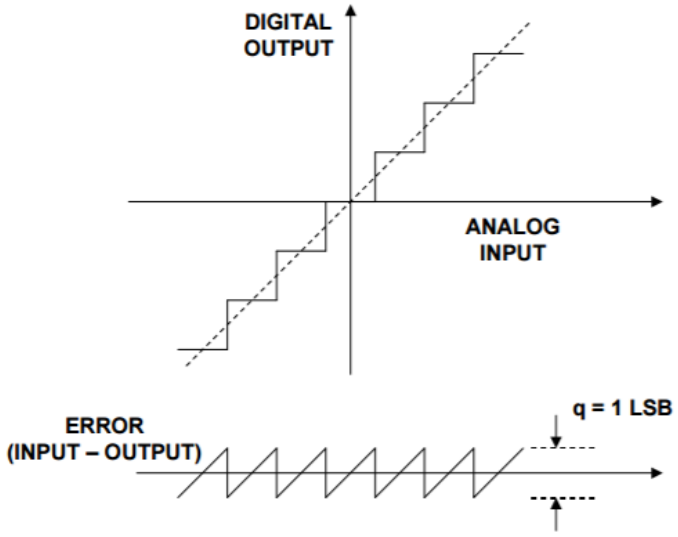


Figure 26. Ideal N-bit ADC quantization noise

The sawtooth error is given by:

$$e(t) = st, -\frac{q}{2s} < t < +\frac{q}{2s} \tag{4.1}$$

And its mean square is:

$$\overline{e^2(t)} = \frac{s}{q}\int_{-q/2s}^{+q/2s} (st)^2 dt \tag{4.2}$$

$$\overline{e^2(t)} = \frac{q^2}{12} \tag{4.3}$$

The RMS of the quantization noise is given by:

$$rms\ quantization\ noise = \sqrt{\overline{e^2(t)}} = \frac{q}{\sqrt{12}} \tag{4.4}$$

The RMS SNR for an ideal N-bit converter is:

$$SNR = 20log\frac{rms\ value\ of\ FS\ input}{rms\ value\ of\ quantization\ noise} \tag{4.5}$$

$$SNR = 20log\left[\frac{q2^N/2\sqrt{2}}{q/\sqrt{12}}\right] = 20log2^N + 20log\sqrt{\frac{3}{2}} \quad (4.6)$$

$$SNR = 6.02N + 1.76dB, from\ DC\ to\frac{f_s}{2}\ bandwidth \quad (4.7)$$

where FS stands for the full scale of the ADC and f_s is the sampling rate ($f_s/2$ is the Nyquist frequency). This expression for SNR, however, considers only the quantization error for an ideal N-bit ADC. To account for distortion, the signal to noise and distortion ratio (SINAD) is used, where the N factor now becomes the effective number of bits (ENOB):

$$SINAD = 6.02(ENOB) + 1.76dB \quad (4.8)$$

The ENOB is commonly found on ADC datasheets. For the MKL25Z128VLK4 microcontroller, the expected ENOB is 11.4. The SINAD is thus:

$$SINAD = 6.02(11.4) + 1.76dB = 70.4dB \quad 4.9)$$

It is then possible to calculate the RMS noise voltage, since the dither magnitude is known:

$$V_{ADCnoise,RMS} = \frac{V_{dither,RMS}}{10^{SINAD/20}} = \frac{3.3V/\sqrt{2}}{3307} = 705.7\mu V \quad (4.10)$$

3. Total RMS noise

Since the two sources of noise are uncorrelated, the total RMS noise is obtained by

$$V_{Totalnoise,RMS} = \sqrt{V_{electricalnoise,RMS}^2 + V_{ADCnoise,RMS}^2} \tag{4.11}$$

$$= \sqrt{(124.9\mu V)^2 + (705.7\mu V)^2}$$

$$= 716.7\mu V$$

In root-sum-of-squares operations the larger value dominates, and so it is evident that the noise from the electrical network is negligible. This means that implementing an electrical network with lower noise would be ineffective in reducing the bias control error.

4. Noise process gain

In digital filter applications where the signal of interest occupies a narrower bandwidth than the Nyquist bandwidth, a correction factor (called process gain) must be included in the equation to account for the resulting increase in SNR (see Figure 27). The process of sampling a signal at a rate which is greater than twice its bandwidth is referred to as oversampling. The expression for SNR is as follows:

$$SNR = 6.02N + 1.76dB + 10log\frac{f_s}{2 \cdot BW} \tag{4.12}$$

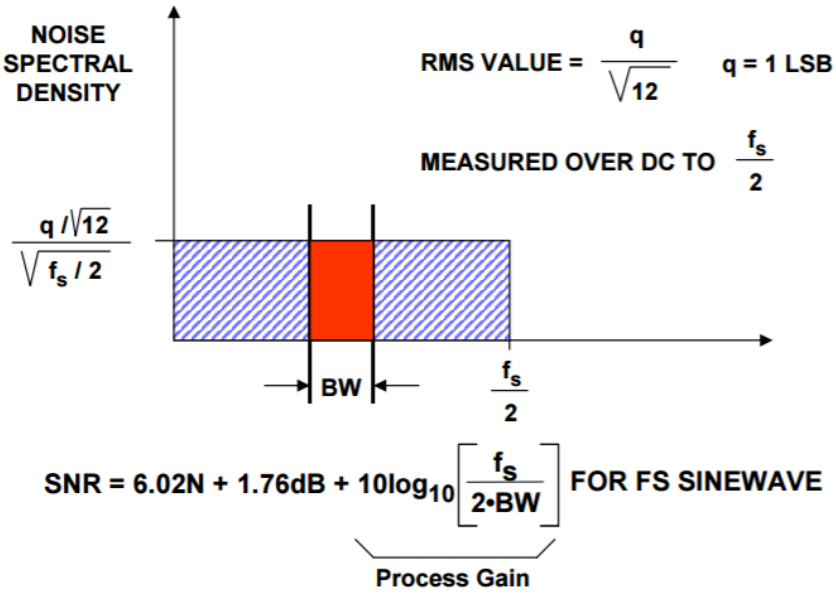


Figure 27. process gain from oversampling and digital filtering on ADC

As depicted in Figure 28, process gain applies also to noise from the electrical network. Only the noise spectrum within the filter passband contributes to the RMS noise at the filter output.

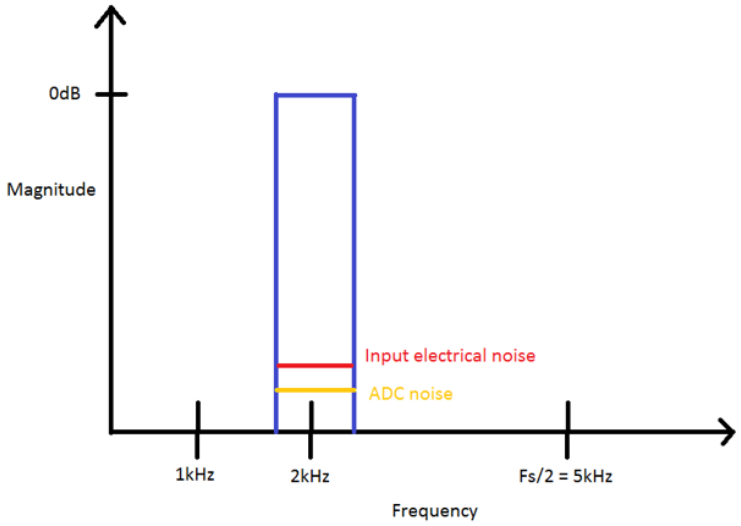


Figure 28. Sources of noise after bandpass digital filter (fc = 2kHz), DC to Nyquist frequency. The filter response is shown in purple.

5. Noise analysis conclusion

The quantization noise analysis and LTSPICE noise simulations indicate that the limited resolution of the ADC is the dominating noise source. It can also be concluded that noise magnitude increases as the digital filter response widens.

5. Digital signal processing and control

A. Digital filter implementations

For the proposed bias control method, the implementation of two bandpass digital filters was necessary to obtain the magnitude and relative phase of each dither signal component.

1. FIR filters

Initially, due to ease of implementation, finite impulse response (FIR) filters were employed. For an N-order FIR filter, the output is a weighted sum of the current input value and the N previous input values, as in:

$$y[n] = b_0 x[n] + b_1 x[n-1] + \cdots + b_N x[n-N] = \sum_{i=0}^{N} b_i \cdot x[n-i] \tag{5.1}$$

This is illustrated in Figure 29, where the z^{-1} operator denotes one unit delay.

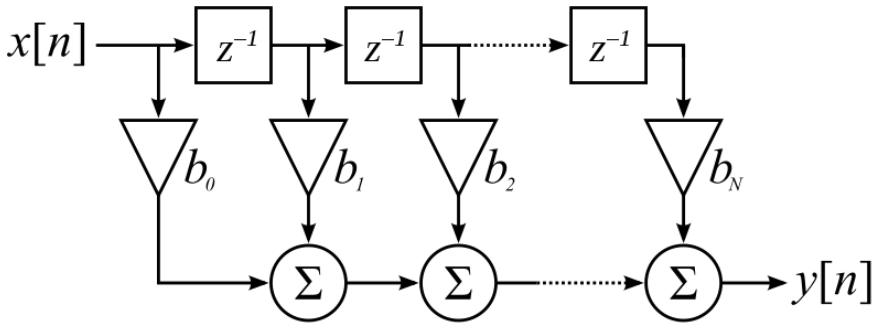


Figure 29. A direct form discrete-time FIR filter of order N

The filters were designed on the MATLAB Filter Designer app, which allows the filter

coefficients to be exported and easily imported to the microcontroller program. Many different filter specifications were tried and the best results were obtained with the 958-tap filter shown in Figure 30. A 1kHz dither frequency and 10kHz ADC sample frequency were chosen. The filter for the 2nd harmonic is equivalent, with the exception that the center of the passband is at 2kHz.

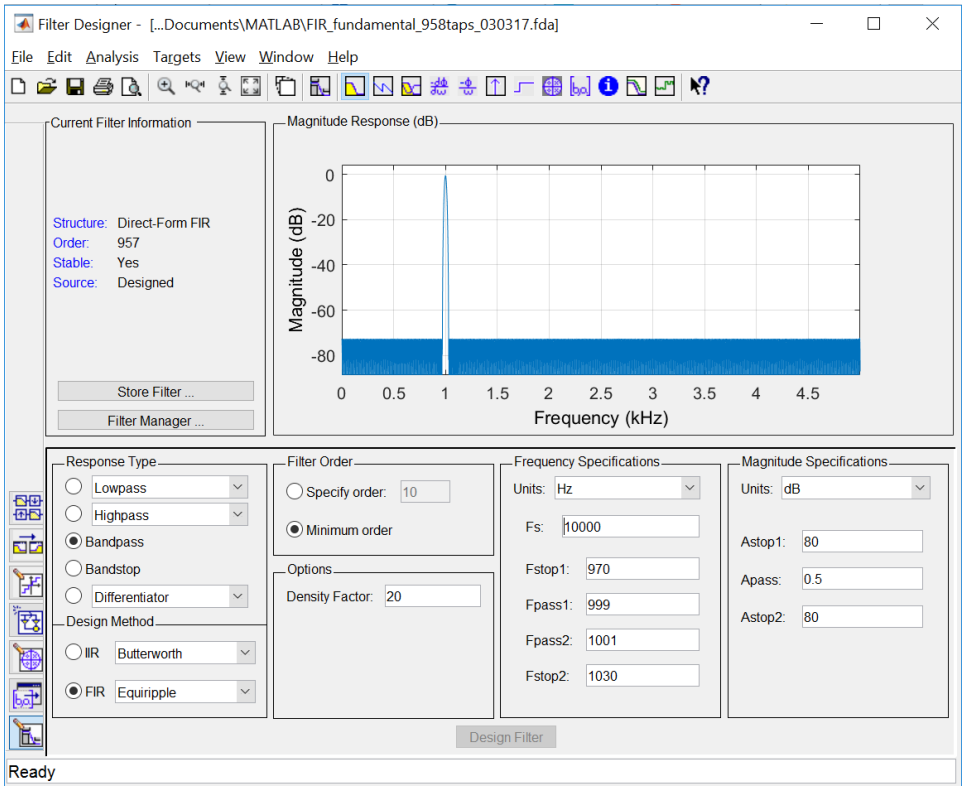


Figure 30. MATLAB Filter Designer, 958-tap FIR filter

Figure 31 shows the bias control measurements vs time (minutes) at quadrature setpoint. The red curve represents the DAC output in volts and the blue curve the ratio of the 2nd to the fundamental dither tones. It can be seen how the DAC voltage increases, slightly overshoots and eventually stabilizes. The ratio drops to the desired setpoint of 0, and has a steady error due to noise. After the PID controller stabilizes, the ratio RMS error is 4.76 x 10^{-4} (-66.4dB),

which corresponds to an average bias error of |0.275°| - i.e., the bias error is a distribution with a mean of 0 and a standard deviation of 0.275°.

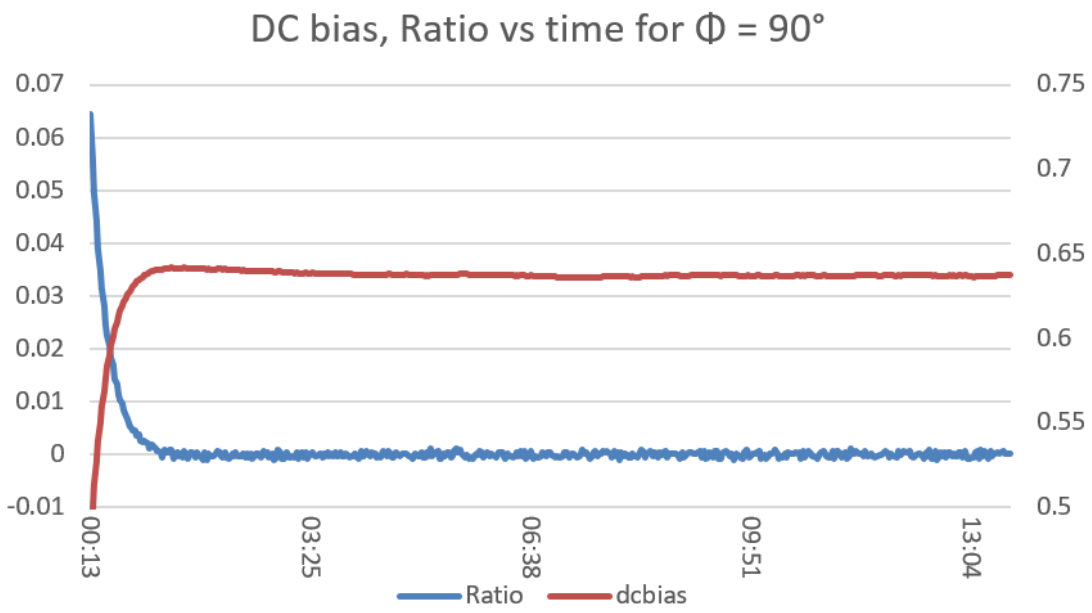


Figure 31. 958-tap FIR filter bias control measurements

Despite obtaining promising results using FIR filters, the large number of taps necessary to achieve a low bias error resulted in a PID loop cycle time of 1.54 seconds. At this point it was decided to apply a different filtering technique to reduce processing time.

2. Correlation receiver

Since only two frequency components need to be measured, correlation is more time-efficient than FIR filtering. As shown in Figure 32, for each frequency it is necessary to correlate with two quadrature signals and then add the time series (integrate). The output is "accumulated and dumped" for a desired number of samples. Both phase and magnitude information can then be obtained from the four summations. The (white) noise will decrease

by $\sqrt{N}$, where N is the number of ADC samples. The bias control measurements using this filtering method are presented in the next chapter.

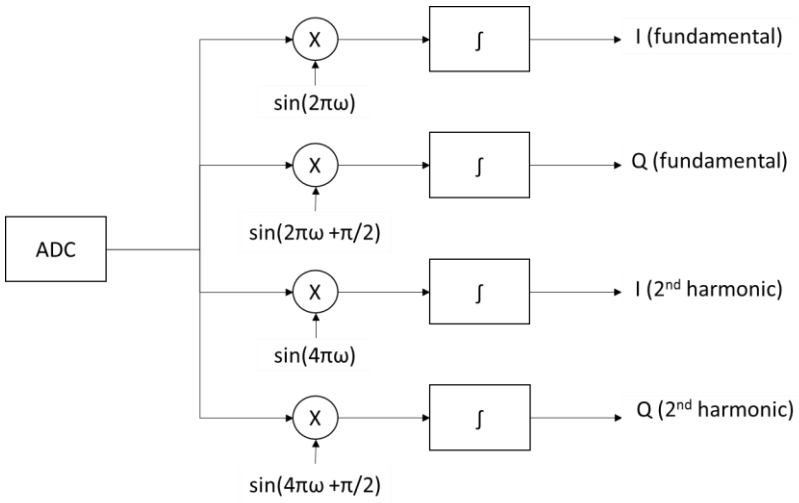


Figure 32. Correlation receiver for dither fundamental and 2nd harmonic

B. PID Control

A PID controller is also implemented within the microcontroller. This control algorithm is the one most commonly used in industry. The popularity of PID controllers can be attributed to their robust performance and functional simplicity. As the name suggests, the PID algorithm consists of three coefficients; proportional, integral and derivative, which are tuned to get optimal response in terms of settling time, overshoot and steady-state error [21]. The variables, as depicted in Figure 33, are as follows:

- Process value: y(t) = Ratio of 2nd harmonic to fundamental
- Control variable: u(t) = DC bias voltage (DAC)
- Setpoint: r(t) = Desired ratio (corresponding to the desired bias point)
- Error: e(t) = Ratio error

- Plant/Process: MZM

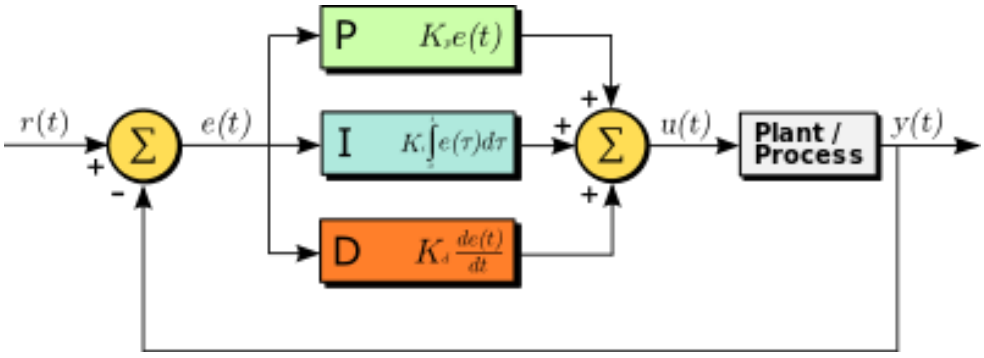


Figure 33. PID controller schematic

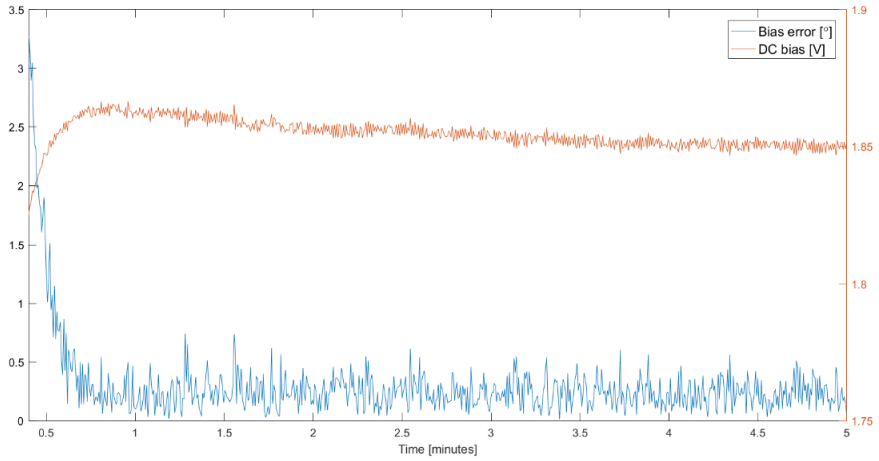
The microcontroller code that contains the correlation receiver and PID controller can be found in Appendix A.

6. Results, further work and conclusion

A. Results

1. Bias control measurements

Bias control measurements were carried out for four different numbers of ADC samples (N) per PID loop cycle. As mentioned above, the MZM V_π is 12V and the 1kHz dither V_p is 2.5V. The setpoint for this experiment is a ratio of 0, which corresponds to quadrature bias, since at this point HD2 should be eliminated. Figure 34 shows the DAC voltage (MZM DC bias) and bias error vs time for N=500, 1500, 2500 and 3500. The ratio calculated within the microcontroller was used to calculate the bias error as in [18]. The PID controller settling time can be noticed at the onset of each test, after which there is a steady error as a consequence of noise, as explained above.



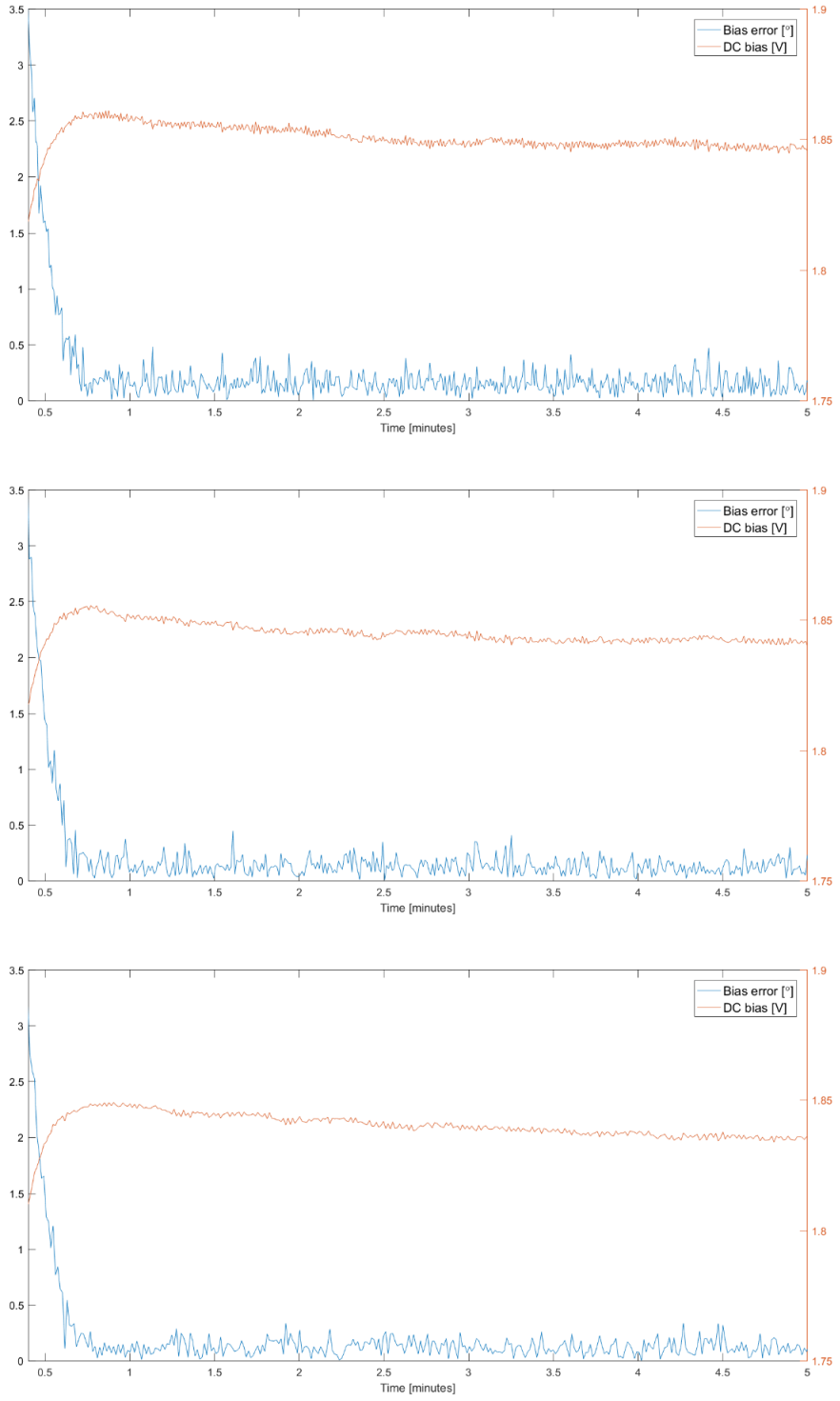


Figure 34. Bias control measurements. From top to bottom: N = 500, 1500, 2500, 3500. The orange curve is the DC voltage value at the DAC output. The blue curve is the bias error in degrees. Setpoint is 90° (quadrature).

A summary of the results is shown in Table 3 and are plotted in Figure 35. It can be observed that as N is increased, the average bias error decreases by $\sqrt{N}$ and the PID cycle time increases linearly. The extrapolated linear time plot intercepts the y-axis at around 0.3 seconds, which can be interpreted as the microcontroller processing time excluding filtering. It is evident that this filtering method is much more time-efficient than using FIR filters, since it requires 0.39 seconds compared to 1.54 seconds for a similar bias error.

Table 3. Bias control measurements summary

N	PID cycle time	Average voltage ratio error	Average power ratio error [dB]	Average absolute bias error [°]
500	0.39	3.76E-04	-68.5	0.26
1500	0.54	2.60E-04	-71.7	0.18
2500	0.68	2.09E-04	-73.6	0.15
3500	0.82	1.95E-04	-74.2	0.14

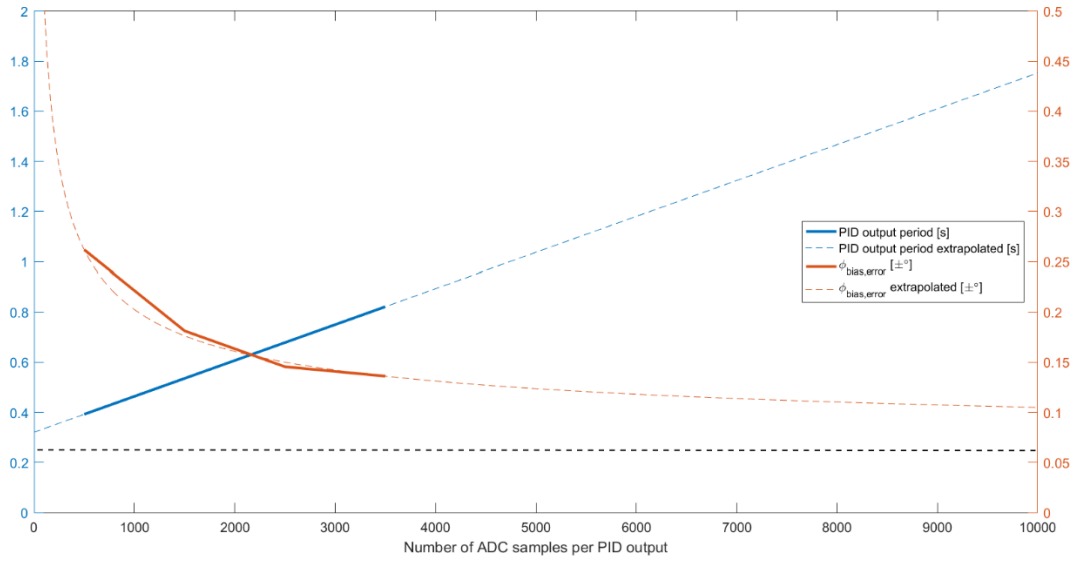


Figure 35. PID output period (loop cycle time) and bias error vs number of ADC samples. The solid orange curve is the measured bias error and the dashed line is the extrapolation. The solid blue line is the PID controller cycle time and the dashed line is the extrapolation.

The bias error extrapolation has an asymptote at 0.06°. This is believed to be caused by

the DAC resolution limit. For an N-bit DAC, the LSB bias phase is:

$$\phi_{LSB} = \frac{\phi_{range}}{2^N - 1} \tag{6.1}$$

Φ_{LSB} is twice the maximum phase error, $\varphi_{error.}$, as can be seen in Figure 36. Approximating for high resolution DACs, N can be expressed by:

$$N = \left[log_2 \left| \frac{\phi_{range}}{2\phi_{error}} + 1 \right| \right] \approx \left[log_2 \left| \frac{\phi_{range}}{\phi_{error}} \right| - 1 \right] \tag{6.2}$$

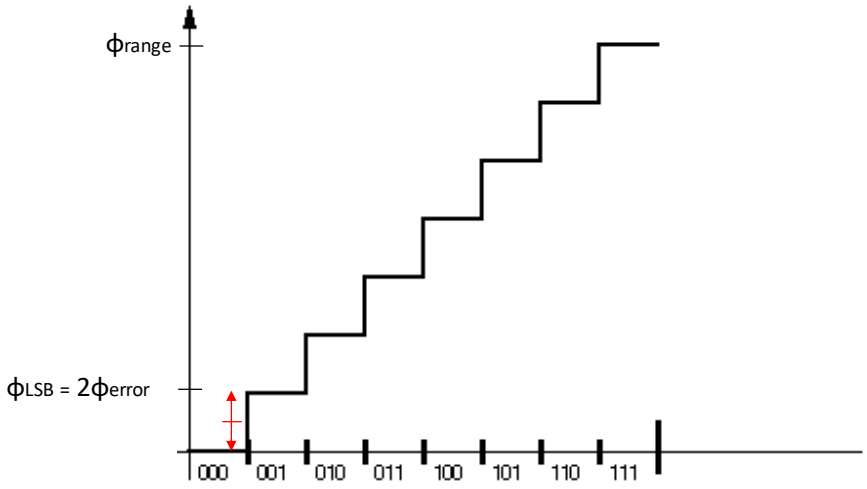


Figure 36. Example of 3-bit DAC with analog phase output vs digital input.

Figure 37 is a plot of the required DAC ENOB vs bias error in degrees for a DAC range of 180° (0 to V_π). The ENOB for 0.06° error is approximately 10.5. This is a reasonable value, considering that the nominal resolution of the microcontroller DAC is 12 bits with ±1-bit differential non-linearity error [22].

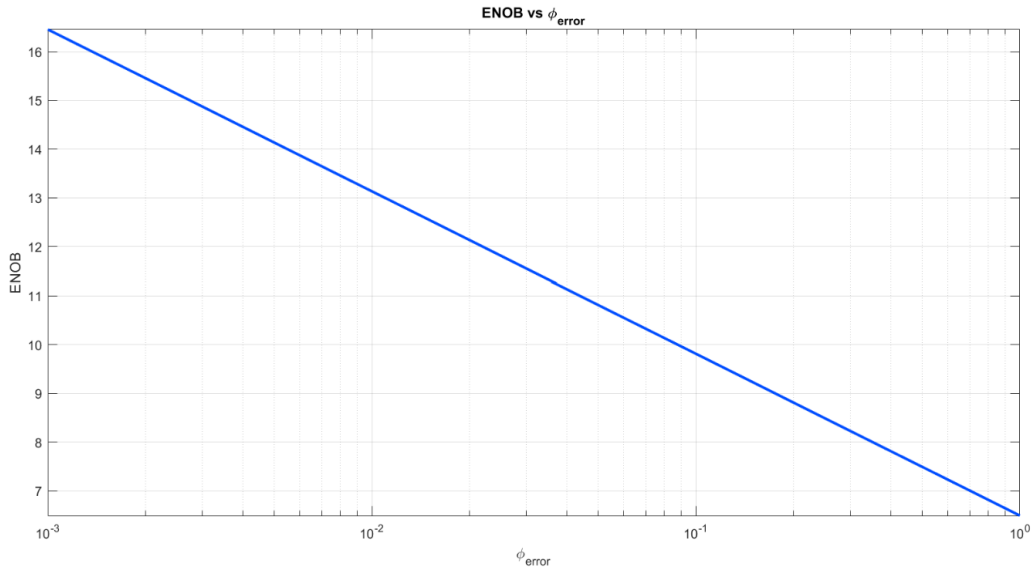


Figure 37. DAC ENOB vs bias error (degrees)

2. HD2, HD3 measurements

2nd and 3rd harmonic distortion measurements were taken at different setpoints to test the modulator bias controller for N=3500. The setup (Figure 38) consisted of the control loop, as well as a variable optical attenuator (VOA) for linearity testing, a power splitter, an analog signal generator (ASG) and an electrical spectrum analyzer (ESA).

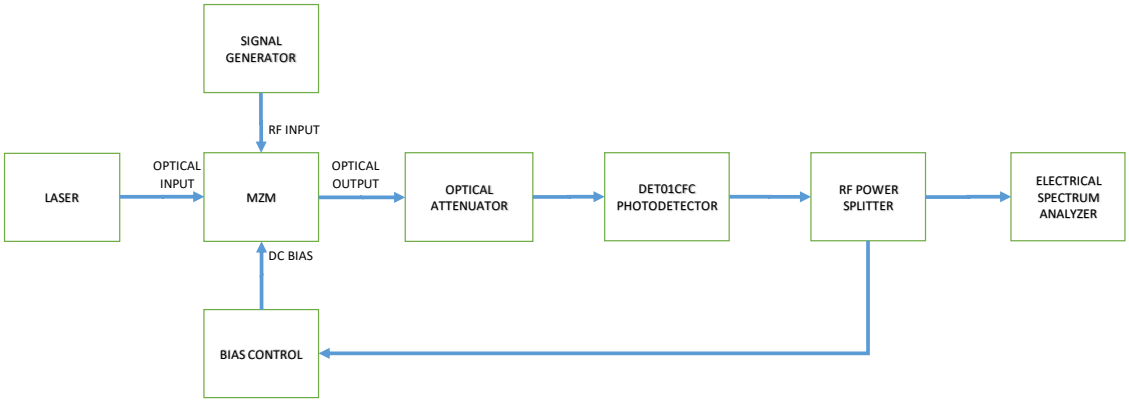


Figure 38. Distortion measurements setup

The linearity of the PD was tested prior to the distortion measurements. A bias point was fixed and the fundamental and 2nd harmonic of an ASG tone were measured. Then, the optical signal was attenuated prior to the PD and the measurements were repeated. The magnitude of both frequencies decreased by the same amount, and thus it was verified that the PD did not introduce additional distortion.

Next, the link's frequency magnitude response (Figure 39) was tested to compensate the HD2 and HD3 for any variations. The relevant bandwidth is 30MHz, since a 10MHz tone was to be input to MZM and the 2nd and 3rd harmonic were to be measured. It can be noted that the magnitude response varies only 1.3dB from 10 to 30MHz. The low bandwidth is attributed to the PD R_L used, which can be adjusted to improve the frequency response if required.

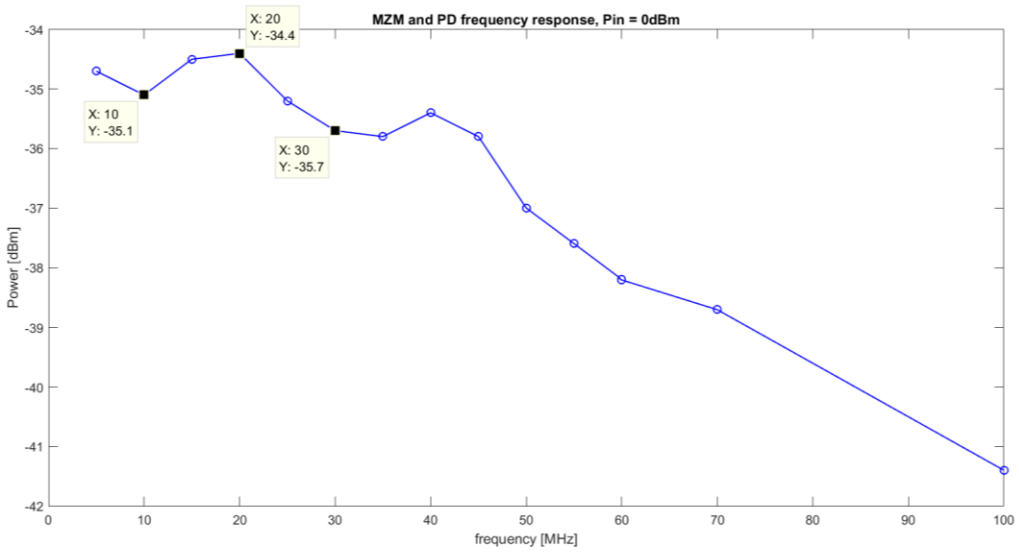


Figure 39. MZM and PD frequency response

A 0dBm 10MHz RF tone and 1.25V 1kHz dither tone were input to the MZM and the bias control setpoint was varied to different bias points. The dither fundamental and HD2, as well as the RF tone fundamental, HD2 and HD3 were measured on the ESA (results in Figure 40). The dither's HD2 to fundamental ratio (74dB) at quadrature setpoint agrees with the results shown above, although there is an offset of approximately 0.5° between setpoint and measured bias point. For the RF tone the ratio is 85dB. As can be seen in the bottom left plot, there is an offset of approximately 1° between the dither signal's and RF tone's quadrature points. The experiment was then repeated for a 500MHz input RF tone (Figure 41). Unfortunately, the HD2 suppression is over 30dB less.

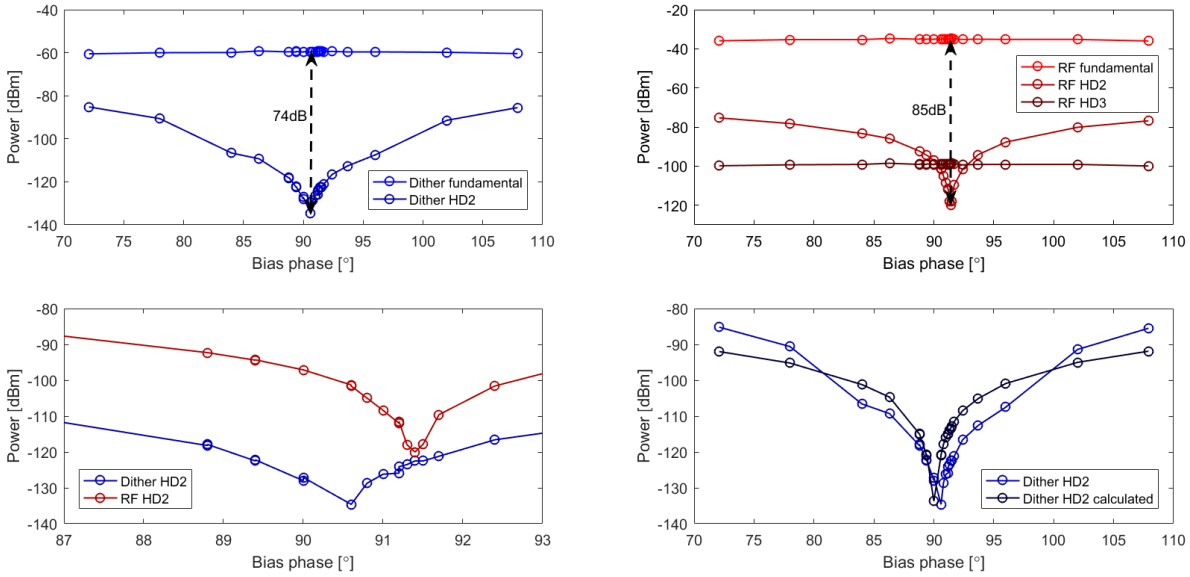


Figure 40. HD2 and HD3 measurements for 10MHz RF tone at different bias setpoints. Dither fundamental and 2nd harmonic, and RF fundamental, 2nd and 3rd harmonics are shown in different plots.

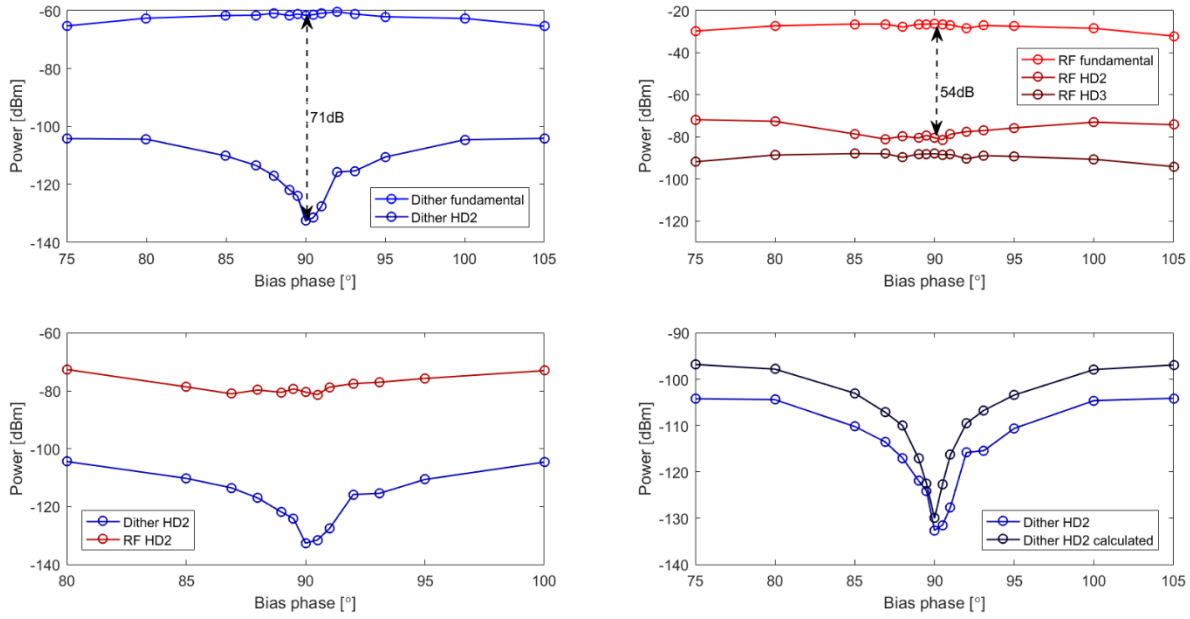


Figure 41. HD2 and HD3 measurements for 500MHz RF tone at different bias setpoints

B. Further work

1. Offset and linearity

The results demonstrate that for the dither signal, the bias control method allows for biasing to different points on the MZM transfer function to within an average error of 0.14° with a PID controller correction time of 0.82s. The correction time increases linearly with the amount of ADC samples, and approximately 10,000 samples would be required to achieve <0.1° average error. This can be achieved with a PID controller correction time of less than 2 seconds, which should be fast enough to compensate the drift in the MZM transfer function. However, there is an observable 0.5° offset between the setpoint and the measured bias point which requires addressing. It is believed that this is an effect of the nonlinearity of the PD load resistor and can be eliminated by employing a transimpedance amplifier (TIA) at the PD output. It is considered that this would also reduce the offset between dither (low-frequency) bias point and RF (high-frequency) bias point, as well as the HD2 values observed for RF tones at quadrature (see Figure 41).

2. Microcontroller with integrated peripherals

There are COTS microcontrollers that incorporate peripherals which can further reduce the number of components used to employ this bias control method. The NXP MCF51MM256/128 (block diagram in Figure 42) has built-in Op Amps and TIAs (TRIAMP). For MZMs with $V_\pi < 3.3V$, in theory only a power supply and the microcontroller would be required to implement the bias control method.

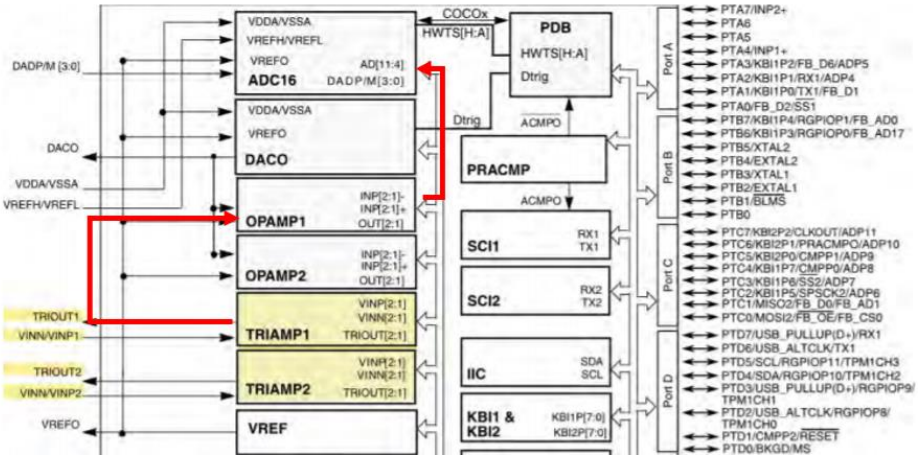


Figure 42. MCF51MM256 series block diagram

3. Application to Si MZM

The main challenge of applying a closed-loop bias control method to Silicon MZMs is that the loss imbalance between the arms is significant, and the transfer function must now be described in terms of a complex effective index [23]. One method that has been simulated utilizes VOAs to produce a "loss dither" in addition to the conventional phase dither used in $LiNbO_3$ MZMs [24]. This provides the spectral information required to determine the imbalance and continually adjust the VOAs. It is the author's opinion that the implementation of that method to the current setup to bias Si MZMs is worth pursuing.

C. Conclusion

A theoretical overview of the MZM was provided and the importance of closed-loop versatile bias control was established. SIMULINK models were then shown for time and frequency-domain analysis. A brief review of MZM bias control patents and publications was then provided. A bias control method with digital filters was proposed to minimize circuit components. The method was then implemented and bias control was tested over time and

distortion measurements were taken at different bias setpoints. In the process, the bias control error due to quantization and electrical noise was analyzed and an expected precision as a function of ADC samples was given. Further work to reduce the offset between setpoint and bias point was discussed, as well as the use of other microcontroller platforms to further simplify the bias control circuit and the potential to extend this method to Si MZMs.

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Appendix A - Microcontroller code

```
#include "mbed.h"
#include "FastAnalogIn.h"


// Tickers, timers - used for ensuring fixed times:
Ticker ADCperiod;     //Creates ticker class "Sampletime" used for ADC conversion
Timer DSPtimer;    //Creates timer class "DSPperiod" used for DSP time.

// Serial communication:
Serial pc(USBTX, USBRX); //tx,rx

//***********************************Pin designations *************************
// ADC pin designation. FastAnalogIn runs ADC in "burst" mode (DMA):
FastAnalogIn adc(PTC2); //float. 0 <=adc <= 1; 0 = 0V, 1.0f = 3.3V
// Other analog inputs are set as digital outputs for better ADC performance:
DigitalOut dig1(PTE22);
DigitalOut dig3(PTE29);
DigitalOut dig4(PTE20);
DigitalOut dig6(PTB0);
DigitalOut dig7(PTB1);
DigitalOut dig8(PTB2);
DigitalOut dig9(PTB3);
DigitalOut dig10(PTC0);
DigitalOut dig11(PTC1);
DigitalOut dig13(PTD1);
DigitalOut dig14(PTD5);
DigitalOut dig15(PTD6);
//DAC pin designation.
AnalogOut dac(PTE30);   //float. 0 <=dac <= 1; 0 = 0V, 1.0f = 3.3V
//*******************************************************************************

//*****************************Constants and variables***************************
//Frequencies and periods:
float sampletime = 0.0001;    //ADC sample time [s]. Should be 1/Fs.
float DACtime = 1;            //DAC time

//Sinewave arguments
int s = 10;                                 //Number of sine arguments
double Sine1_I[] = {0.000000000000000E+00,5.877852522924730E-01,9.510565162951540E-
01,9.510565162951540E-01,5.877852522924730E-01,1.225148454908620E-16,-5.877852522924730E-01,-
9.510565162951540E-01,-9.510565162951540E-01,-5.877852522924730E-01};
double Sine1_Q[] = {1.000000000000000E+00,8.090169943749470E-01,3.090169943749480E-01,-
3.090169943749470E-01,-8.090169943749470E-01,-1.000000000000000E+00,-8.090169943749480E-01,-
3.090169943749480E-01,3.090169943749470E-01,8.090169943749470E-01};
double Sine2_I[] = {0.000000000000000E+00,9.510565162951540E-01,5.877852522924730E-01,-
5.877852522924730E-01,-9.510565162951540E-01,-2.450296909817240E-16,9.510565162951540E-
01,5.877852522924730E-01,-5.877852522924730E-01,-9.510565162951540E-01};
double Sine2_Q[] = {1.000000000000000E+00,3.090169943749480E-01,-8.090169943749470E-01,-
8.090169943749480E-01,3.090169943749470E-01,1.000000000000000E+00,3.090169943749480E-01,-
8.090169943749470E-01,-8.090169943749480E-01,3.090169943749470E-01};

//ADC parameters:
int N = 3500;         //Number of samples per DSP cycle. Must be a multiple of s.
int c;                //Ratio of number of samples to sinewave arguments
float ADC_Array[3500];       //serves as a shift register for the ADC conversions.

//Correlation:
double Sn1_I, Sn1_Q, Sn2_I, Sn2_Q;
```

```
float pi = 3.14;
double Mag_fund, Mag_2nd, Phase_fund, Phase_2nd;
double ratio, phase;

//PID controller:
double dspsampletime;                   //Stores PID sample size
double setpoint = 0;        //PID controller set point. 0 for quadrature.
double Kp = 1, Ki= 0.5, Kd= 0.1;        //PID coefficients
double Pout, Iout, Dout;                //PID outputs
double loop_error, pre_error, errormin = 1e5;      //PID errors
double PIDoutput = 0.5;                                     //PID output. DAC output.
double max = 0.85, min = 0.15;          //PID output minimum and maximum values

//Auxiliary constants
int j, k, l; //used as a counters in for loops
//*********************************************************************************


//Function that moves adc value to shift register. Repeats every sample time:
void ADC_register(){
   if (j < N){
      ADC_Array[j] = adc;
      j++;
      }
   }

//Correlation
void Correlation(){
   Sn1_I = 0;
   Sn1_Q = 0;
   Sn2_I = 0;
   Sn2_Q = 0;
   for (k = 0; k < c; k++){
      for (l = 0; l < s; l++){
         Sn1_I += ADC_Array[s*k+l] * Sine1_I[l];
         Sn1_Q += ADC_Array[s*k+l] * Sine1_Q[l];
         Sn2_I += ADC_Array[s*k+l] * Sine2_I[l];
         Sn2_Q += ADC_Array[s*k+l] * Sine2_Q[l];
         }
      }
   Mag_fund = sqrt(Sn1_I*Sn1_I + Sn1_Q*Sn1_Q);
   Mag_2nd = sqrt(Sn2_I*Sn2_I + Sn2_Q*Sn2_Q);
   Phase_fund = atan2(Sn1_Q,Sn1_I);
   Phase_2nd = atan2(Sn2_Q,Sn2_I);
   phase = 2*Phase_fund - Phase_2nd;
   if ((phase >= (-3*pi) && phase < (-2*pi)) || (phase >= (-
pi) && phase < 0) || (phase >= pi && phase < (2*pi))){
      ratio = -Mag_2nd / Mag_fund;
      }
      else{
         ratio = Mag_2nd / Mag_fund;
         }
}

//PID controller:
void PID_control(){
   loop_error = setpoint - ratio;   // Calculate error
   if (abs(loop_error) < errormin){
      loop_error = 0;
      }
   Pout = Kp * loop_error;  // Proportional
```

```
111.    Iout += Ki*(loop_error + pre_error)* 0.5 * dspsampletime;   //Integral
112.    Dout = Kd*(loop_error - pre_error) / dspsampletime; // Derivative
113.    PIDoutput = Pout + Iout + Dout; // Calculate total output
114.    if( PIDoutput > max ){ // Restrict to max/min
115.       PIDoutput = max;
116.       }
117.       else if( PIDoutput < min ){
118.          PIDoutput = min;
119.          }
120.    dac = PIDoutput;    //0 <= biasdc <= 1; 0.0 = 0V, 1.0f = 3.3V
121.    pre_error = loop_error; // Save error to previous error
122.    }
123.
124.
125. int main() {
126.
127.    ADCperiod.attach(&ADC_register, sampletime);  //Attaches ticker to ADC_read function with a fixed sample
       time "sampletime"
128.
129.    c = N/s;
130.
131.    while(1) {
132.
133.          if(j == N){  //After ADC values are obtained, dsptime is calculated for PID controller:
134.             dspsampletime = DSPtimer.read();
135.             DSPtimer.reset();
136.             DSPtimer.start();
137.
138.             Correlation();
139.
140.             PID_control();
141.
142.             pc.printf("{TIMEPLOT:Ratio plot|data|Ratio|T|%E}\n",ratio);
143.             pc.printf("{TIMEPLOT:Ratio plot|data|dcbias|T|%E}\n",PIDoutput);
144.             pc.printf("{TIMEPLOT:Ratio plot|set|title=Ratio}\n");
145.             pc.printf("{TIMEPLOT:Ratio plot|set|x-label=Time}\n");
146.             pc.printf("{TIMEPLOT:Ratio plot|set|y-label=Ratio}\n");
147.
148.             wait(0.1);
149.
150.             j = 0;
151.
152.             }
153.
154.    }
155.
156. }
```